1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
B		358902	PRODUCTION RELEASED	01/07/05	?

SCHEM,MLB,PB15"
01/07/2005

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1	TITLE PAGE AND CONTENTS
2	SYSTEM BLOCK DIAGRAM
3	POWER BLOCK DIAGRAM
4	PCB NOTES AND HOLES
5	MPC7447A MAXBUS INTERFACE
6	MPC7447A DATA/NC PINS/BOOTBANGER
7	CPU PLL AND CONFIGURATION STRAPS
8	INTREPID MAXBUS AND BOOT STRAPS
9	INTREPID MEMORY INTERFACE/BOOTROM
10	DDR MEMORY MUXES
11	400PIN STACKED DDR SODIMM CONNECTOR
12	INTREPID AGP 4X/PCI
13	INTREPID ENET/FW/UATA/EIDE INTERFACES
14	INTREPID GPIOS/SERIAL/USB INTERFACES/SSCG
15	INTREPID POWER RAILS/1.5V LDO
16	INTREPID DECOUPLING
17	USB 2.0 INTERFACE (uPD720101)
18	CARDBUS INTERFACE (PCI1510)
19	M11 AGP INTERFACE & SPREAD SPECTRUM
20	EXTERNAL TMDS (DUAL TMDS - SIL178)
21	M11 LVDS/TMDS/GPIO & GPU VCORE
22	M11 POWER

PAGE	CONTENTS
23	VIDEO CONNECTORS - INVERTER,DVI, LVDS,S-VIDEO
24	SPIDEY,PWR BUTTON,ALS
25	MMM & BATTERY CURRENT SENSE CIRCUIT
26	INTERNAL CONNECTORS-AIRPORT,HDD,ODD
27	FAN CONTROLLER,SW MODEM,SERIAL DEBUG SOUND/LEFT USB/BLUETOOTH
28	GIGABIT ETHERNET INTERFACE
29	FIREWIRE PHY
30	FIREWIRE PORTS
31	PMU
32	BATTERY CHARGER AND CONNECTOR
33	PBUS SUPPLY,PMU SUPPLY,SUPERCAP ,BACKUP BATTERY
34	3.3V/5V SYSTEM POWER SUPPLY
35	CPU CORE VOLTAGE POWER SUPPLY
36	1.5V/1.8V/2.5V SYS. POWER SUPPLIES
37	SIGNAL CONSTRAINTS(PG1)-DDR MEM/CLK
38	SIGNAL CONSTRAINTS(PG2)-CPU
39	SIGNAL CONSTRAINTS(PG3)-DIGITAL/DIFF
40	SIGNAL CONSTRAINTS(PG4)-POWER NETS
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42	REVISION HISTORY
43-46	SCHEMATIC CREF AND NETLIST REPORTS

BOM OPTIONS (IN COMMON PARTS)

STUFF	NO STUFF
1_8V_MAXBUS	1_5V_MAXBUS
NO_SSCG	SSCG
5V_HD_LOGIC	3V_HD_LOGIC
NO_BBANG	BBANG
INT_2_5V_COLD	INT_2_5V_HOT
ATI_MEMIO_HI	ATI_MEMIO_LO
SOFT_MODEM	USB_MODEM
GPU_PWRMSR	EMI
GPU_SS	EXT_TMDS (BETTER/BEST)
VGA_BUFFER_RES	INT_TMDS (BEST128)
MMM	SUPERCAP
INT_TMDS (BETTER/BEST)	ADT7460
EXT_TMDS (BEST128)	
BACKUP_BATT	
ADT7467	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6680	1	SCHEM,MLB,PB15	SCH1	
820-1679	1	PCBF,MLB,PB15	PCB1	

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE NONE	

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

Apple Computer Inc.

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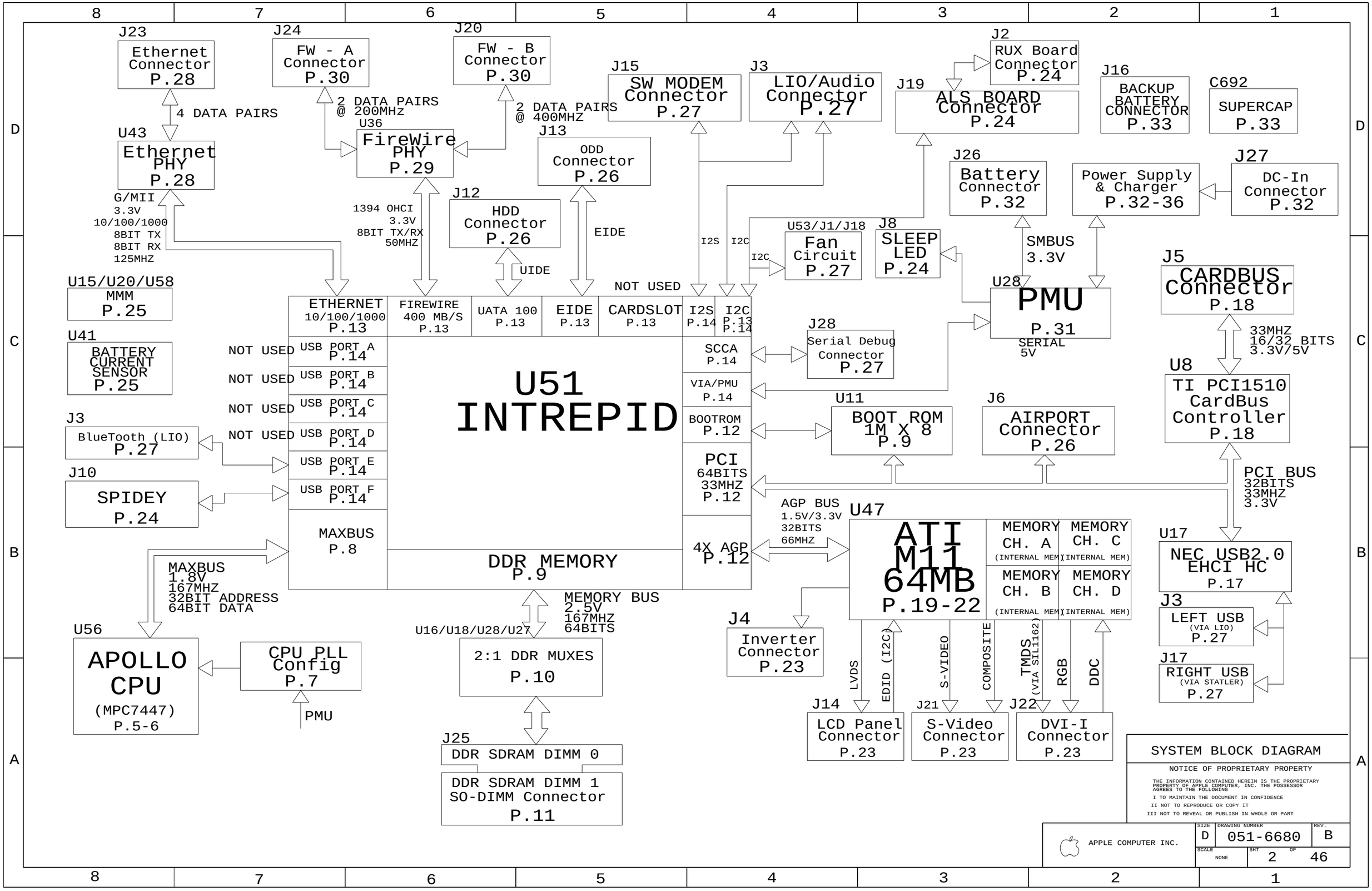
TITLE
SCHEM,MLB,PB15

DRAWING NUMBER 051-6680 REV. B


J23
Ethernet Connector P.28
J24
FW - A Connector P.30
J20
FW - B Connector P.30
J15
SW MODEM Connector P.27
J3
LIO/Audio Connector P.27
J2
RUX Board Connector P.24
J19
ALS BOARD Connector P.24
J16
BACKUP BATTERY CONNECTOR P.33
C692
SUPERCAP P.33
4 DATA PAIRS
2 DATA PAIRS @ 200MHz
2 DATA PAIRS @ 400MHZ
U36
FireWire PHY P.29
J13
ODD Connector P.26
U43
Ethernet PHY P.28
G/MII
3.3V
10/100/1000
8BIT TX
8BIT RX
125MHZ
1394 OHCI
3.3V
8BIT TX/RX
50MHZ
J12
HDD Connector P.26
EIDE
UIDE
J26
Battery Connector P.32
Power Supply & Charger P.32-36
J27
DC-In Connector P.32
U53/J1/J18
Fan Circuit P.27
J8
SLEEP LED P.24
I2S
I2C
SMBUS
3.3V
U15/U20/U58
MMM P.25
NOT USED
ETHERNET 10/100/1000 P.13
FIREWIRE 400 MB/S P.13
UATA 100 P.13
EIDE P.13
CARDSLOT P.13
I2S P.14
I2C P.13 P.14
U28
PMU P.31
SERIAL
5V
J5
CARDBUS Connector P.18
33MHZ
16/32 BITS
3.3V/5V
U41
BATTERY CURRENT SENSOR P.25
NOT USED
USB PORT A P.14
USB PORT B P.14
USB PORT C P.14
USB PORT D P.14
USB PORT E P.14
USB PORT F P.14
U51
INTREPID
SCCA P.14
VIA/PMU P.14
BOOTROM P.12
PCI 64BITS 33MHZ P.12
4X AGP P.12
J28
Serial Debug Connector P.27
U8
TI PCI1510 CardBus Controller P.18
U11
BOOT ROM 1M X 8 P.9
J6
AIRPORT Connector P.26
J3
BlueTooth (LIO) P.27
J10
SPIDEY P.24
PCI BUS
32BITS
33MHZ
3.3V
AGP BUS
1.5V/3.3V
32BITS
66MHZ
U47
ATI M11 64MB P.19-22
MEMORY CH. A (INTERNAL MEM)
MEMORY CH. C (INTERNAL MEM)
MEMORY CH. B (INTERNAL MEM)
MEMORY CH. D (INTERNAL MEM)
U17
NEC USB2.0 EHCI HC P.17
MAXBUS P.8
DDR MEMORY P.9
MAXBUS
1.8V
167MHZ
32BIT ADDRESS
64BIT DATA
MEMORY BUS
2.5V
167MHZ
64BITS
J3
LEFT USB (VIA LIO) P.27
J17
RIGHT USB (VIA STATLER) P.27
U56
APOLLO CPU (MPC7447) P.5-6
CPU PLL Config P.7
PMU
U16/U18/U28/U27
2:1 DDR MUXES P.10
J4
Inverter Connector P.23
LVDS
EDID (I2C)
S-VIDEO
COMPOSITE
TMDS (VIA SIL1162)
RGB
DDC
J14
LCD Panel Connector P.23
J21
S-Video Connector P.23
J22
DVI-I Connector P.23
J25
DDR SDRAM DIMM 0
DDR SDRAM DIMM 1
SO-DIMM Connector P.11
SYSTEM BLOCK DIAGRAM
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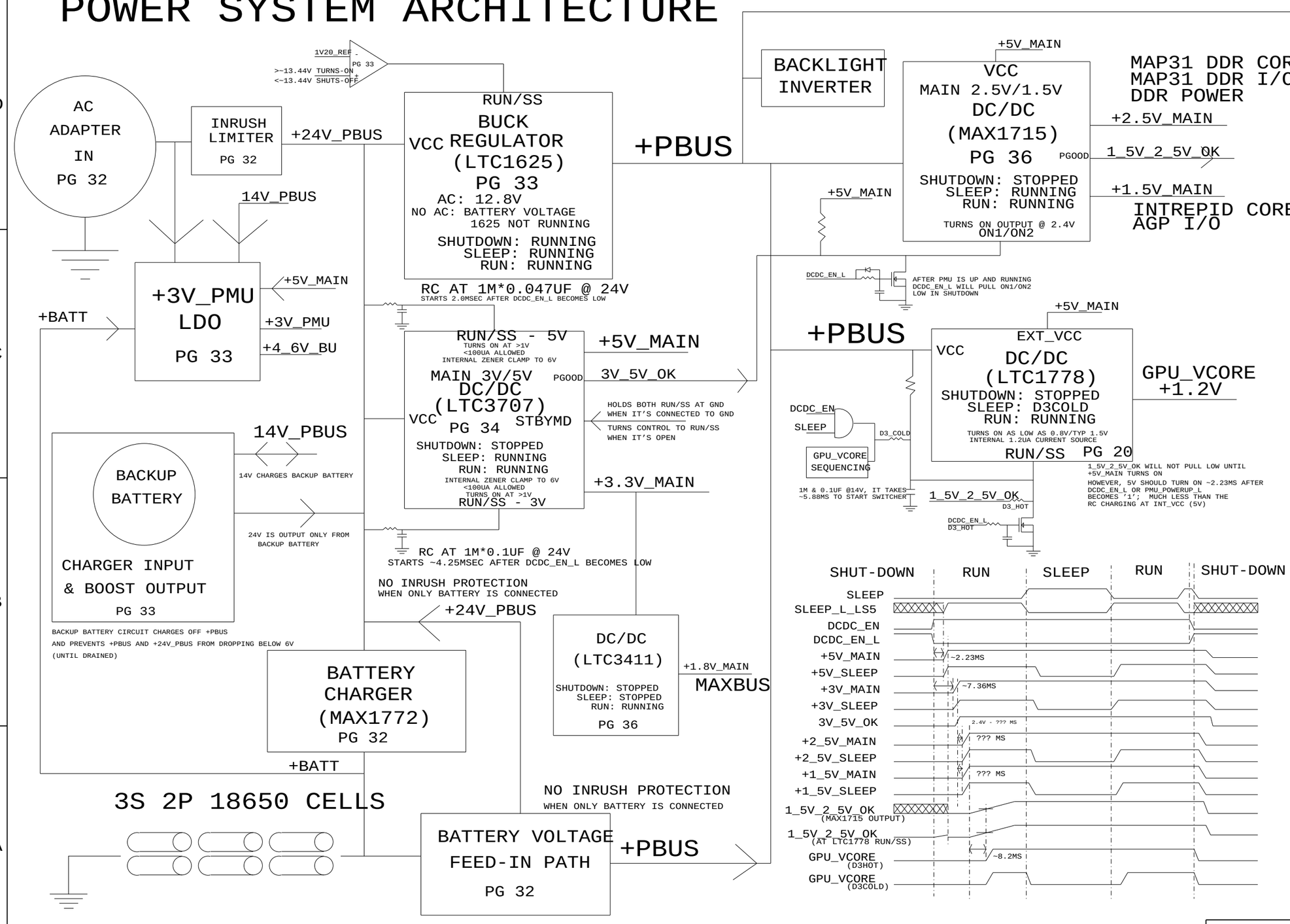
SIZE D
DRAWING NUMBER 051-6680
REV. B
SCALE NONE
SHT 2 OF 46

POWER SYSTEM ARCHITECTURE



POWER BLOCK DIAGRAM

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SIZE	DRAWING NUMBER	REV.
D	051-6680	B
SCALE NONE	SHT 3 OF 46	

PCB SPECS

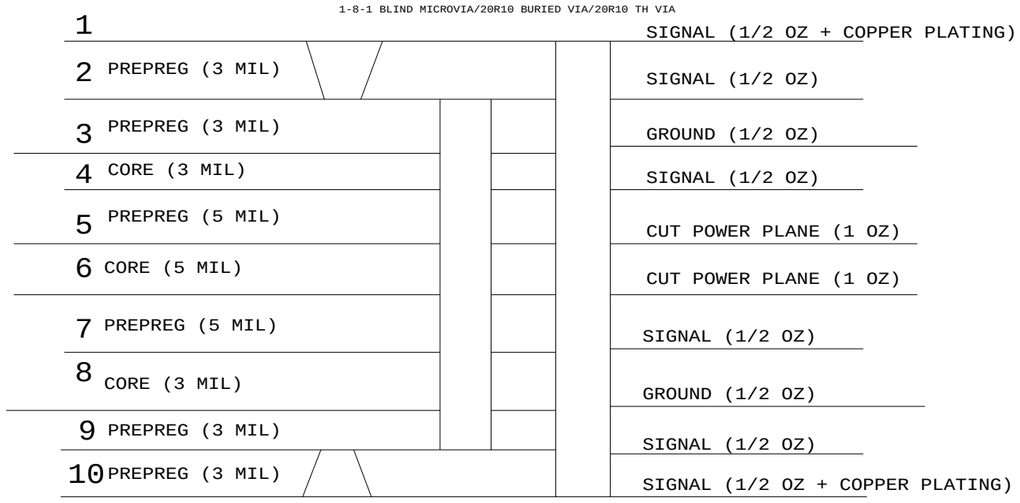
THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 10
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

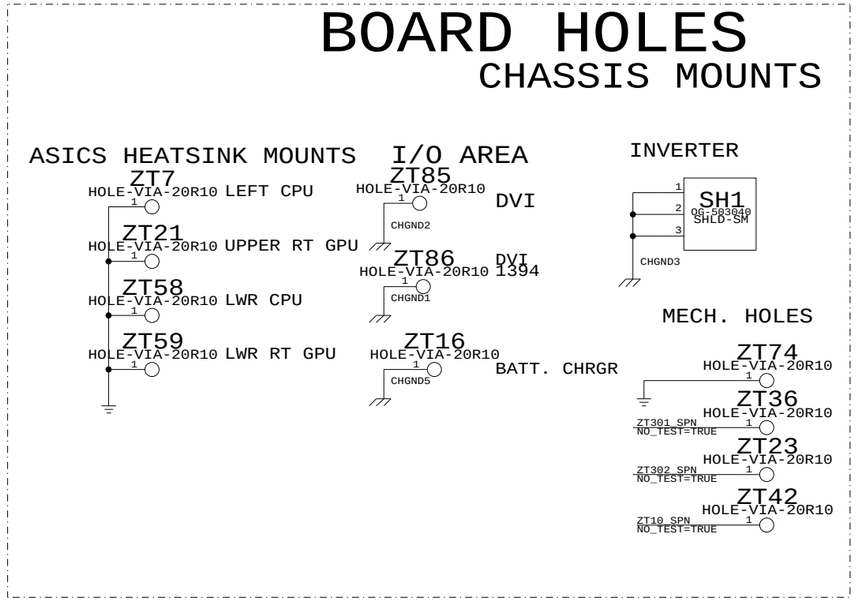
BOARD STACK-UP AND CONSTRUCTION

1-8-1 BLIND MICROVIA/20R10 BURIED VIA/20R10 TH VIA

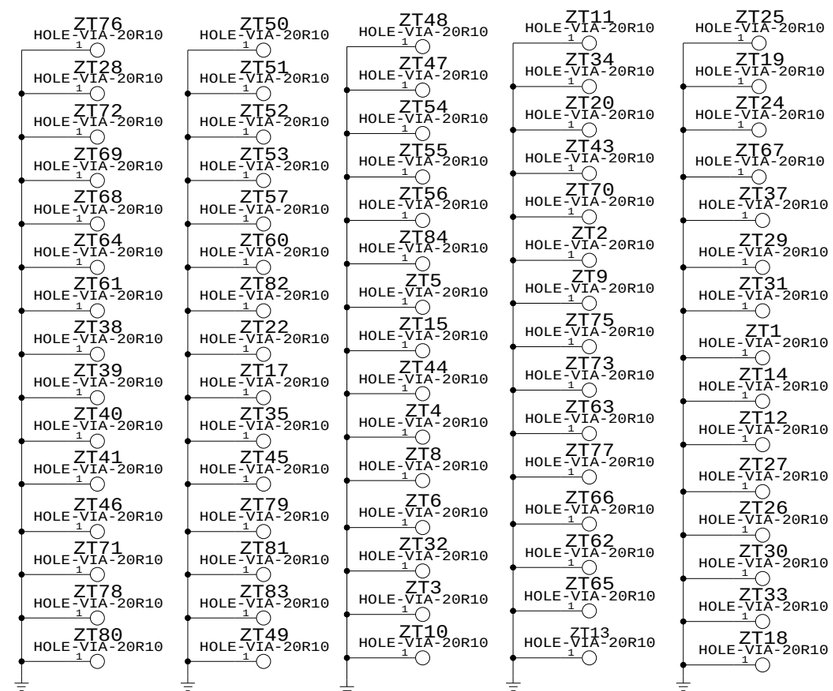


BOARD HOLES

CHASSIS MOUNTS



GROUND VIAS



BOARD INFORMATION

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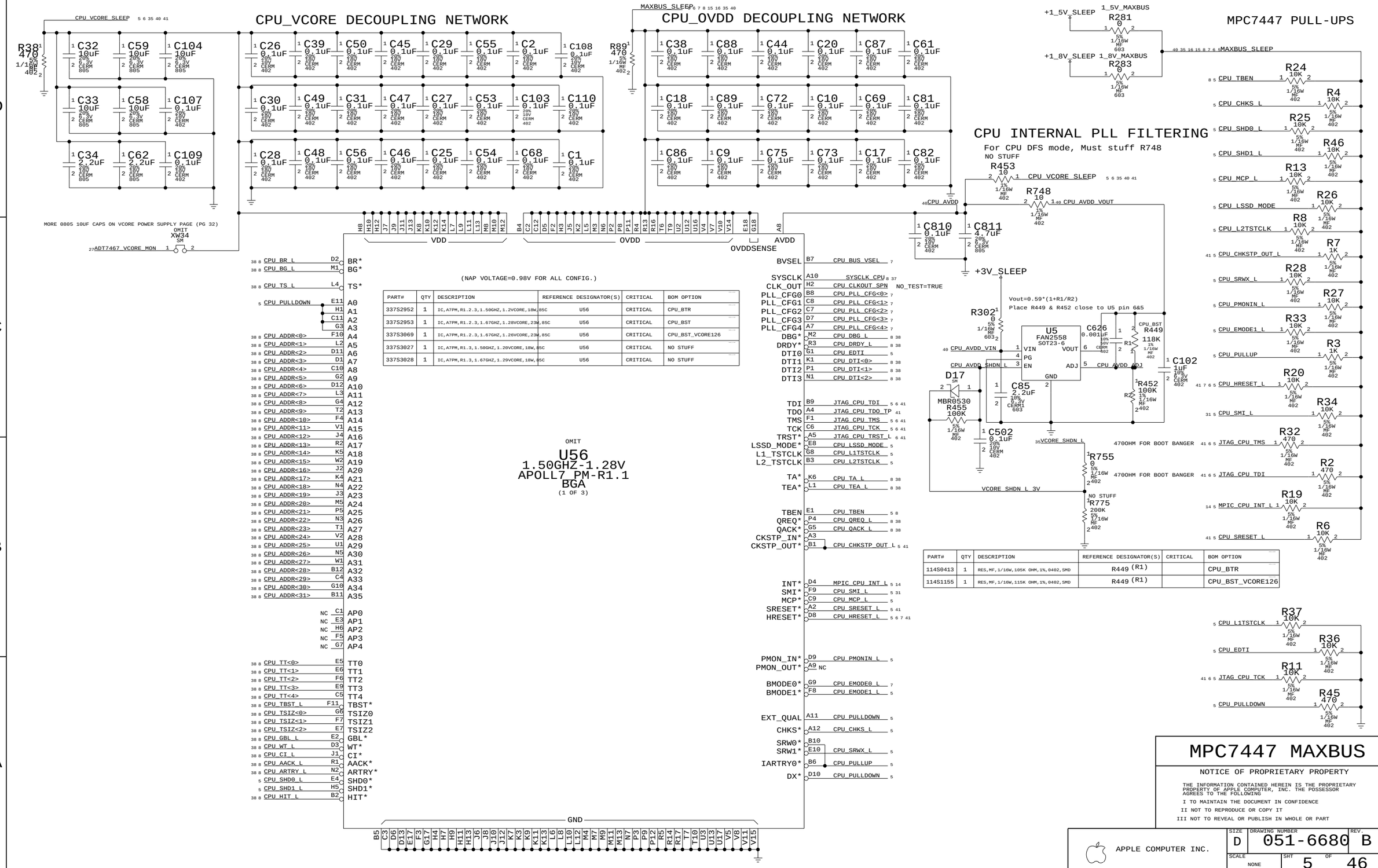
SCALE NONE	SHT 4 OF 46	


CPU_VCORE DECOUPLING NETWORK
CPU_OVDD DECOUPLING NETWORK
MPC7447 PULL-UPS
CPU INTERNAL PLL FILTERING
For CPU DFS mode, Must stuff R748
NO STUFF
MORE 0805 10uF CAPS ON VCORE POWER SUPPLY PAGE (PG 32)
(NAP VOLTAGE=0.98V FOR ALL CONFIG.)
U56
1.50GHZ-1.28V
APOLL7_PM-R1.1
BGA
(1 OF 3)
Vout=0.59*(1+R1/R2)
Place R449 & R452 close to U5 pin 6&5
470OHM FOR BOOT BANGER
MPC7447 MAXBUS
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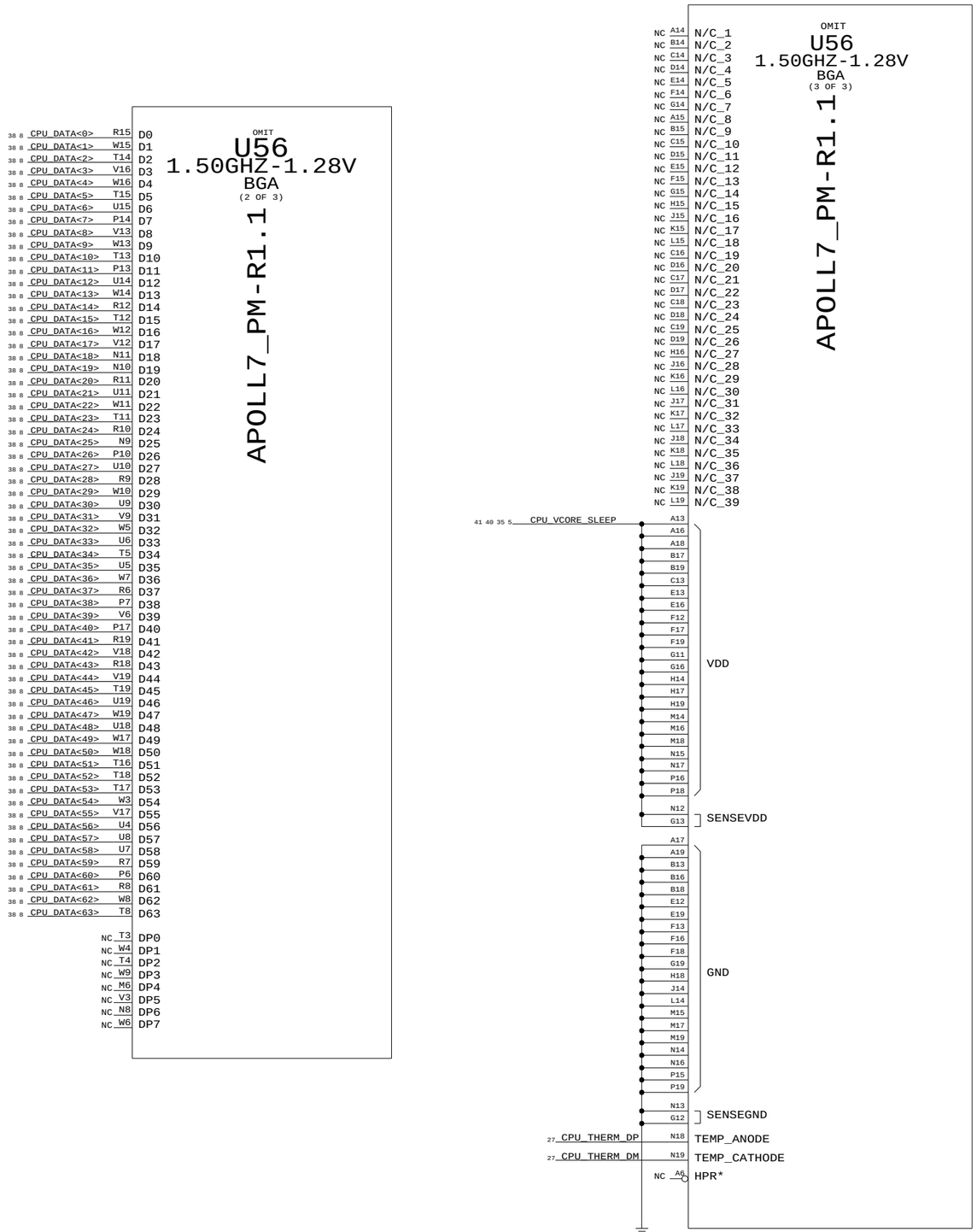
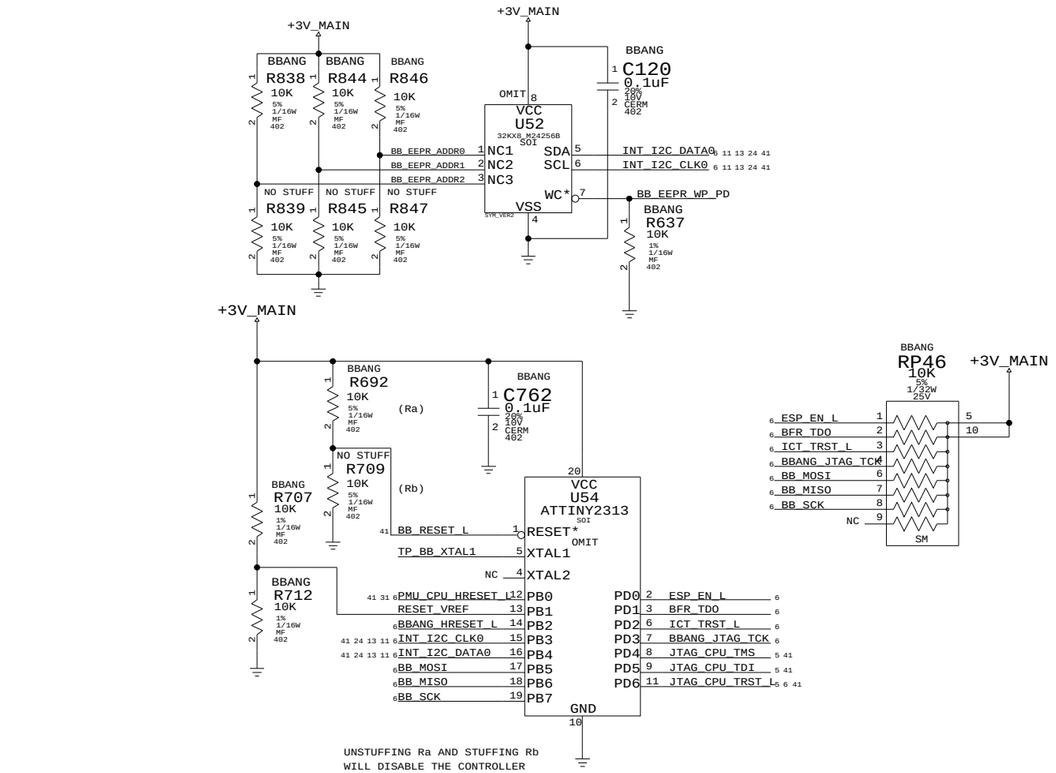
SHT 5 OF 46



BOOT BANGER - TWEAK PROCESSOR BITS AFTER POWER-ON



UNSTUFFING Ra AND STUFFING Rb
WILL DISABLE THE CONTROLLER

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1660	1	MCU,PROGRAMMED W/ BBANGER	U54	BBANG
341S1661	1	I2C EEPROM,PROGRAMMED W/ BBANGER	U52	BBANG

MPC7447/BBANG

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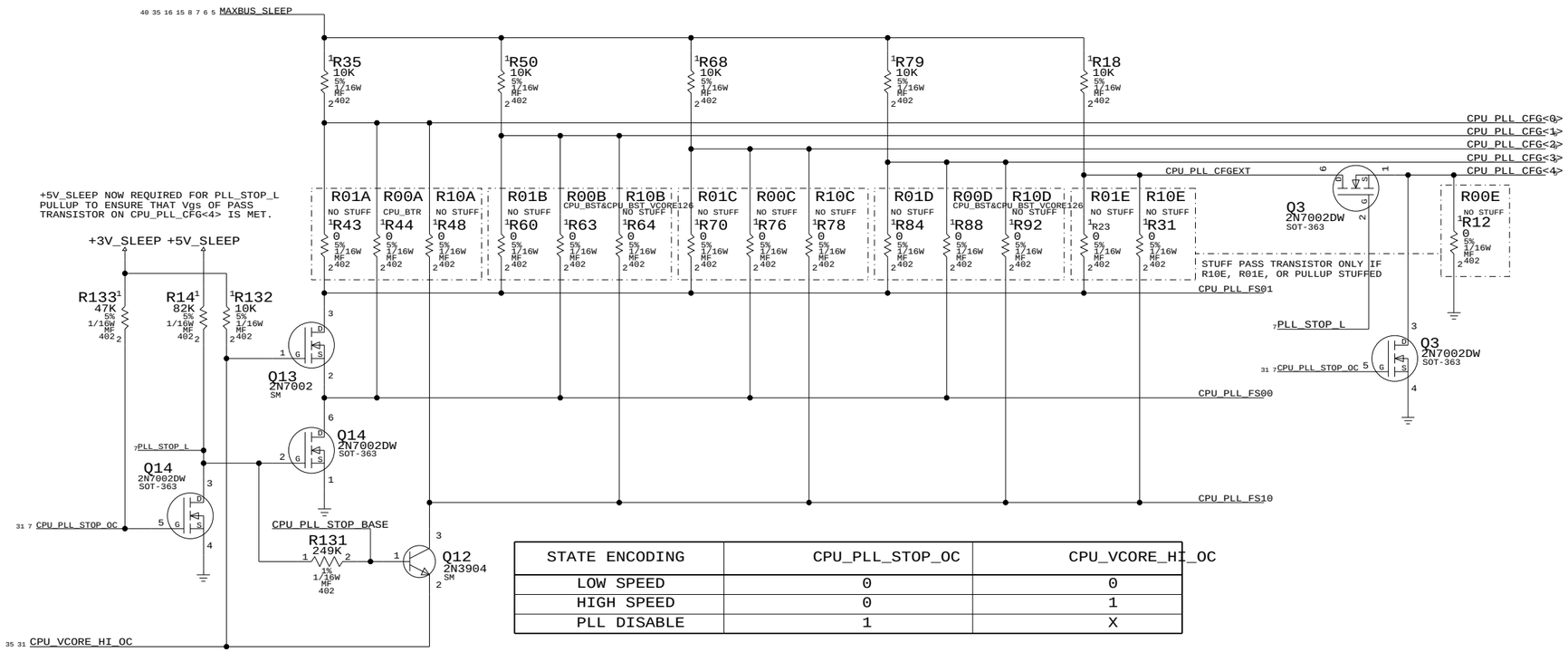
SIZE	DRAWING NUMBER	REV.
D	051-6680	B
SCALE NONE	SHT 6 OF 46	

CPU PLL CONFIG CIRCUITRY



STATE ENCODING	CPU_PLL_STOP_OC	CPU_VCORE_HI_OC
LOW SPEED	0	0
HIGH SPEED	0	1
PLL DISABLE	1	X

CPU FREQUENCY CONFIGURATION

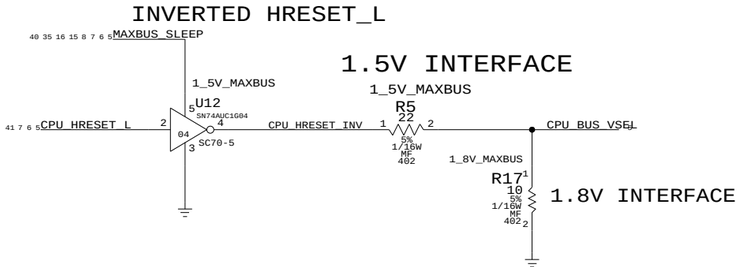
APOLLO 7PM

MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY) (MHZ) 167MHZ	133MHZ	CPU_PLL_CFG 4 E	0123 ABCD HEX
0.0X	PLL OFF		0	1111 0F
1.0X	PLL BYPASS		0	0011 03
2.0X	333	267	0	0100 04
3.0X	500	400	0	1000 08
4.0X	667	533	0	1010 0A
5.0X	833	667	0	1011 0B
5.5X	917	733	0	1001 09
6.0X	1000	800	0	1101 0D
6.5X	1083	867	0	0101 05
7.0X	1167	933	0	0010 02
7.5X	1250	1000	0	0001 01
8.0X	1333	1067	0	1100 0C
8.5X	1417	1133	0	0110 06
9.0X	1500	1200	1	0111 17
9.5X	1583	1267	0	0111 07
10.0X	1667	1333	1	1010 1A
10.5X	1750	1400	1	1000 18
11.0X	1833	1467	1	1001 19
11.5X	1917	1533	0	0000 00
12.0X	2000	1600	1	1011 1B
12.5X	2083	1667	1	1111 1F
13.0X	2167	1733	1	0101 15
13.5X	2250	1800	0	1110 0E
14.0X	2333	1867	1	1100 1C
15.0X	2500	2000	1	0001 11
16.0X	2667	2133	1	1101 1D
17.0X	2833	2267	1	0000 10
18.0X	3000	2400	1	0010 12
20.0X	3333	2667	1	0011 13
21.0X	3500	2800	1	0100 14
24.0X	4000	3200	1	0110 16
28.0X	4667	3733	1	1110 1E

CPU CONFIGURATION

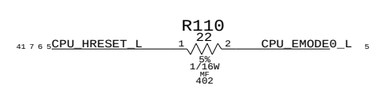
MAXBUS VSEL

INVERTED HRESET_L



DESKTOP HAD PROBLEM USING INVERTER TO INVERT HRESET_L NEED TO CHARACTERIZE

BUSTYPE SELECT



APOLLO ONLY SUPPORTS MAXBUS

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

CPU CONFIGURATION

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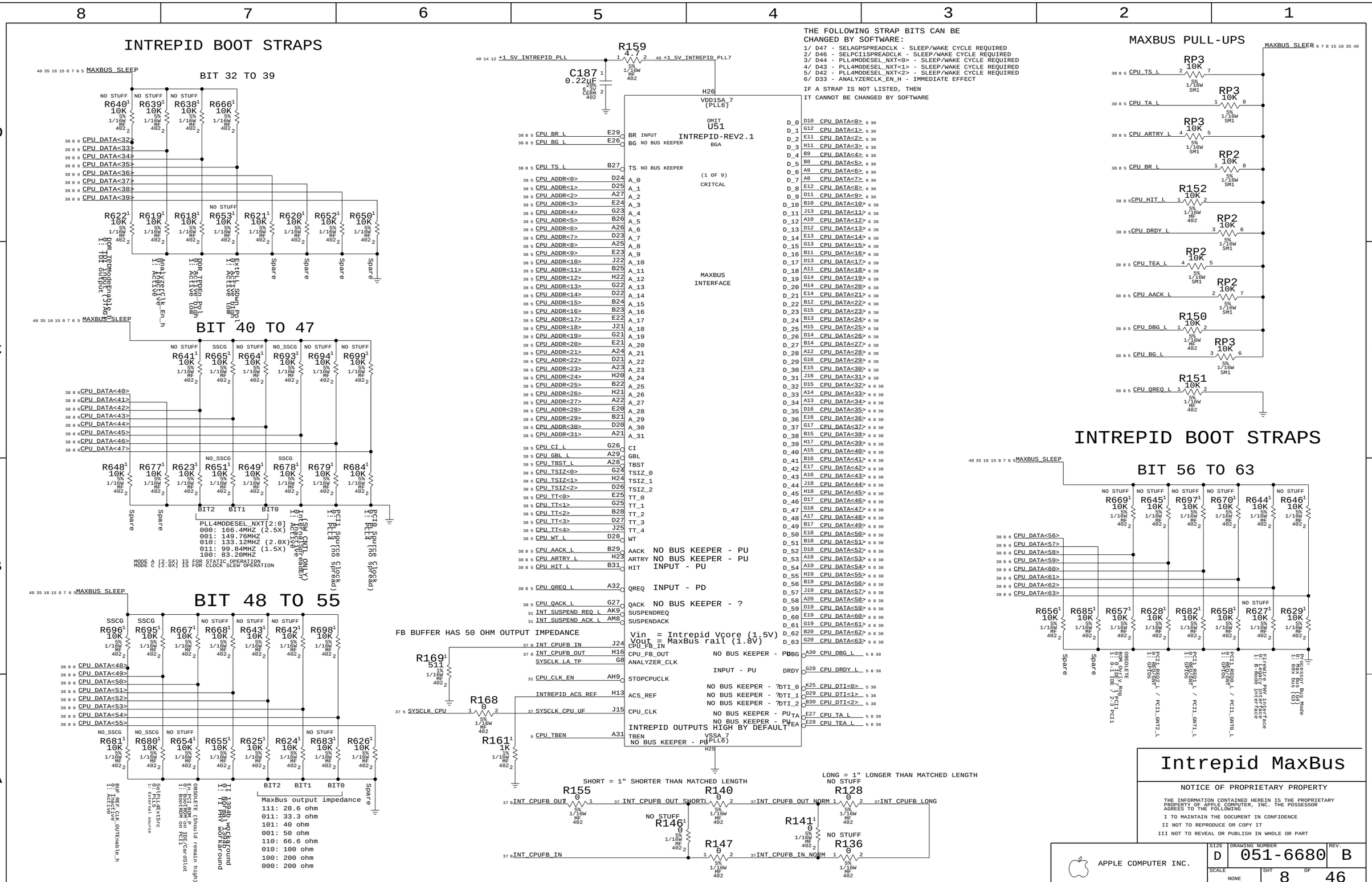
INTREPID BOOT STRAPS
BIT 32 TO 39
BIT 40 TO 47
BIT 48 TO 55
MAXBUS SLEEP
PLL4MODESEL_NXT[2:0]
000: 166.4MHZ (2.5X)
001: 149.76MHZ
010: 133.12MHZ (2.0X)
011: 99.84MHZ (1.5X)
100: 83.20MHZ
MODE A (2.5X) IS FOR STATIC OPERATION
MODE C (2.0X) IS FOR CLOCK SLEW OPERATION
MaxBus output impedance
111: 28.6 ohm
011: 33.3 ohm
101: 40 ohm
001: 50 ohm
110: 66.6 ohm
010: 100 ohm
100: 200 ohm
000: 200 ohm
FB BUFFER HAS 50 OHM OUTPUT IMPEDANCE
INTREPID OUTPUTS HIGH BY DEFAULT
THE FOLLOWING STRAP BITS CAN BE CHANGED BY SOFTWARE:
1/ D47 - SELAGPSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
2/ D46 - SELPCI1SPREADCLK - SLEEP/WAKE CYCLE REQUIRED
3/ D44 - PLL4MODESEL_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
4/ D43 - PLL4MODESEL_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
5/ D42 - PLL4MODESEL_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
6/ D33 - ANALYZERCLK_EN_H - IMMEDIATE EFFECT
IF A STRAP IS NOT LISTED, THEN
IT CANNOT BE CHANGED BY SOFTWARE
INTREPID-REV2.1
BGA
(1 OF 9)
CRITCAL
MAXBUS INTERFACE
MAXBUS PULL-UPS
INTREPID BOOT STRAPS
BIT 56 TO 63
SHORT = 1" SHORTER THAN MATCHED LENGTH
LONG = 1" LONGER THAN MATCHED LENGTH
Intrepid MaxBus
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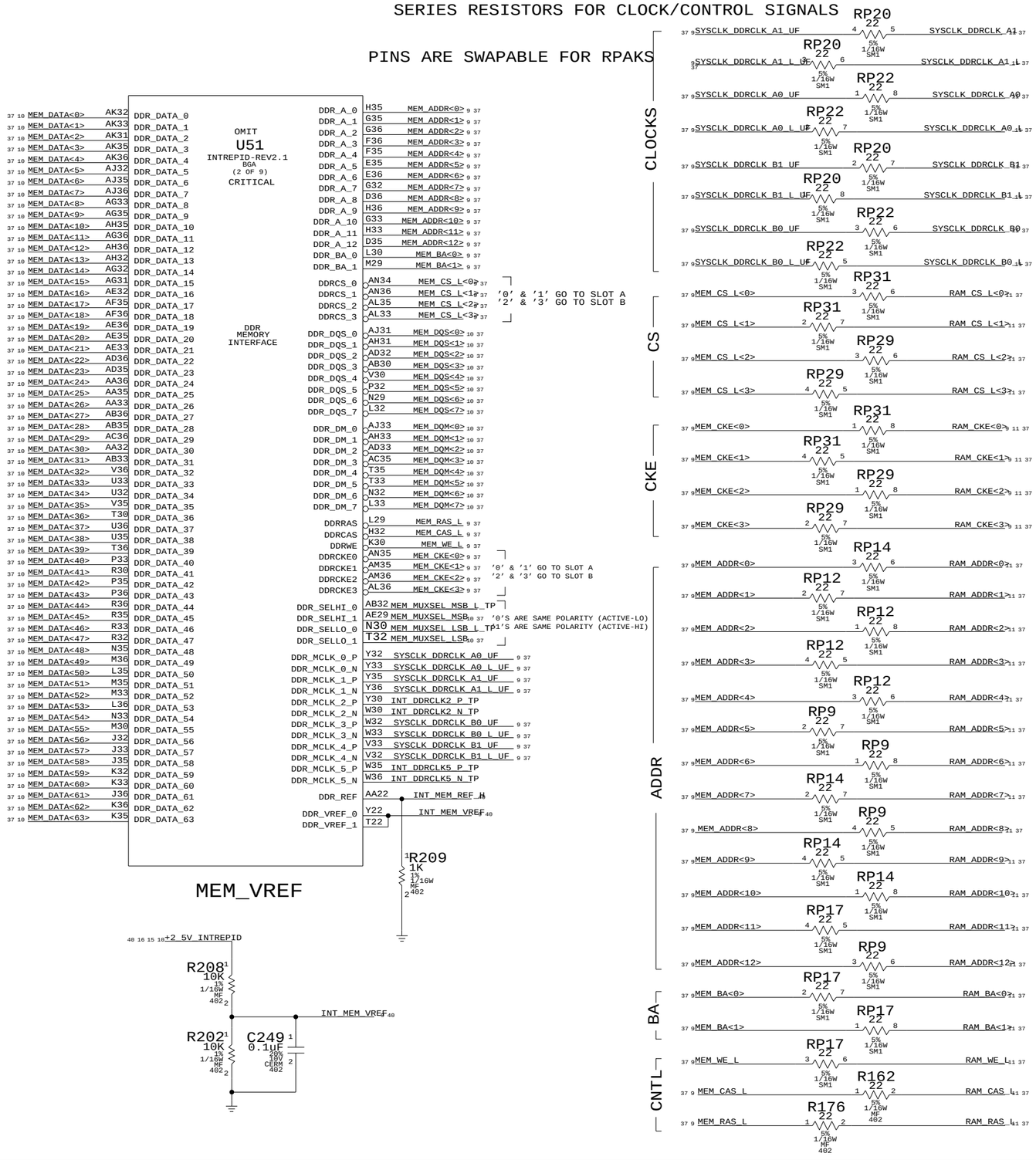
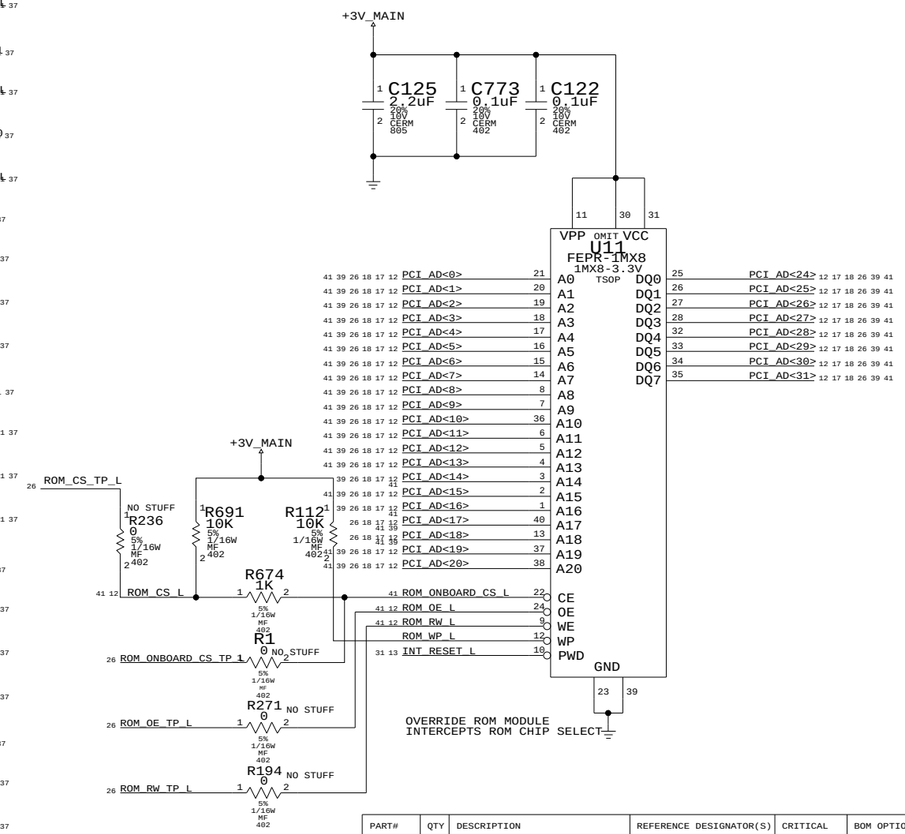
SIZE D
DRAWING NUMBER 051-6680
REV. B
SCALE NONE
SHT 8 OF 46

SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS

PINS ARE SWAPABLE FOR RPAKS

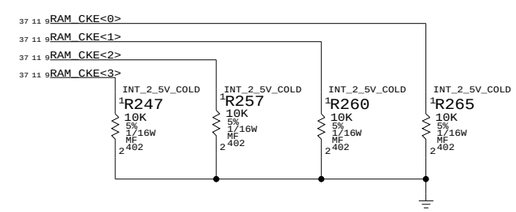


1MB BOOT ROM



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1555	1	IC,BOOTROM Q16B	U11	CRITICAL	?

Weak pulldowns ensure CKEs stay low
after 2.5V I/O to Intrepid shuts off.



INT - DDR/BOOTROM

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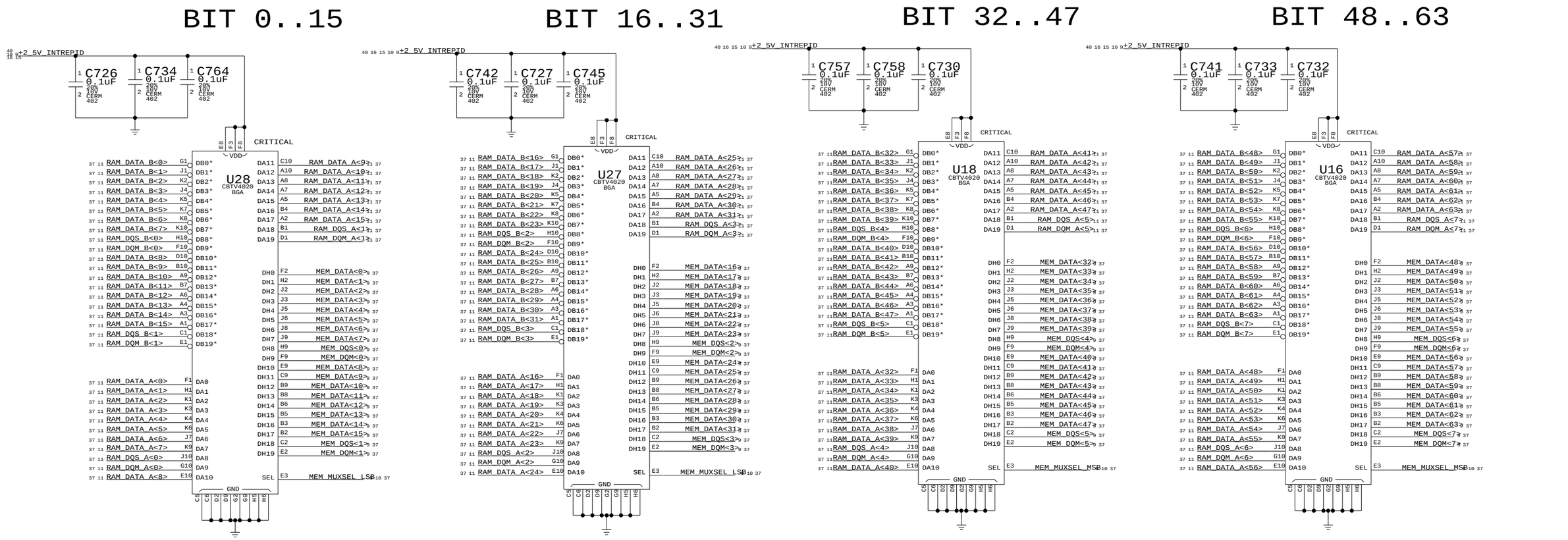
SIZE	DRAWING NUMBER	REV.
D	051-6680	B
SCALE NONE	SHT 9 OF 46	



SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND

16BIT 2:1 DDR MUXES

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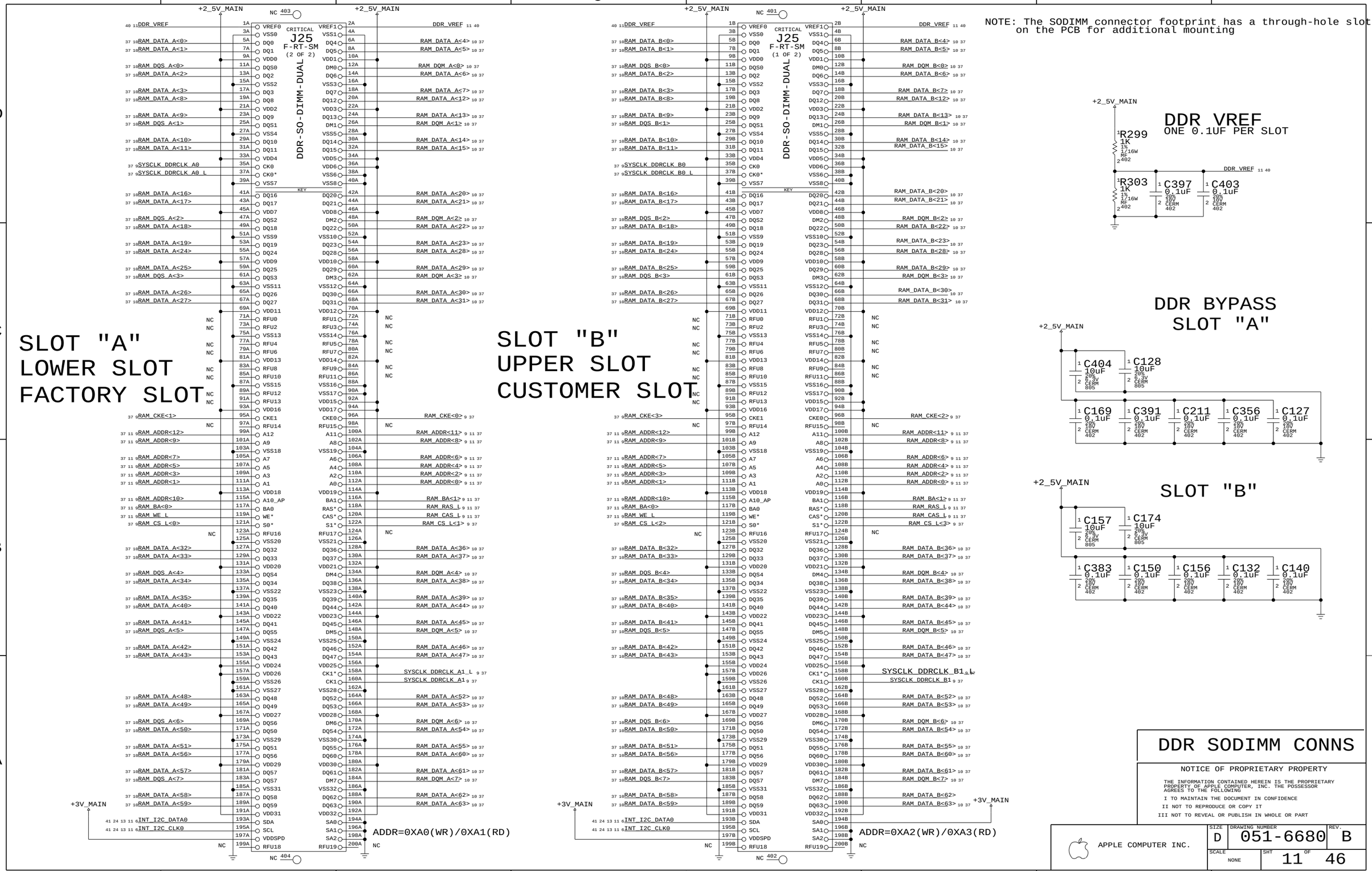
D	051-6680	B
SCALE NONE	SHT 10 OF 46	


SLOT "A"
LOWER SLOT
FACTORY SLOT
J25
F-RT-SM
(2 OF 2)
CRITICAL
DDR-SO-DIMM-DUAL
KEY
ADDR=0XA0(WR)/0XA1(RD)
SLOT "B"
UPPER SLOT
CUSTOMER SLOT
J25
F-RT-SM
(1 OF 2)
ADDR=0XA2(WR)/0XA3(RD)
NOTE: The SODIMM connector footprint has a through-hole slot on the PCB for additional mounting
DDR VREF
ONE 0.1UF PER SLOT
R299 1K
R303 1K
C397 0.1uF
C403 0.1uF
DDR BYPASS
SLOT "A"
C404 10uF
C128 10uF
C169 0.1uF
C391 0.1uF
C211 0.1uF
C356 0.1uF
C127 0.1uF
SLOT "B"
C157 10uF
C174 10uF
C383 0.1uF
C150 0.1uF
C156 0.1uF
C132 0.1uF
C140 0.1uF
DDR SODIMM CONNS
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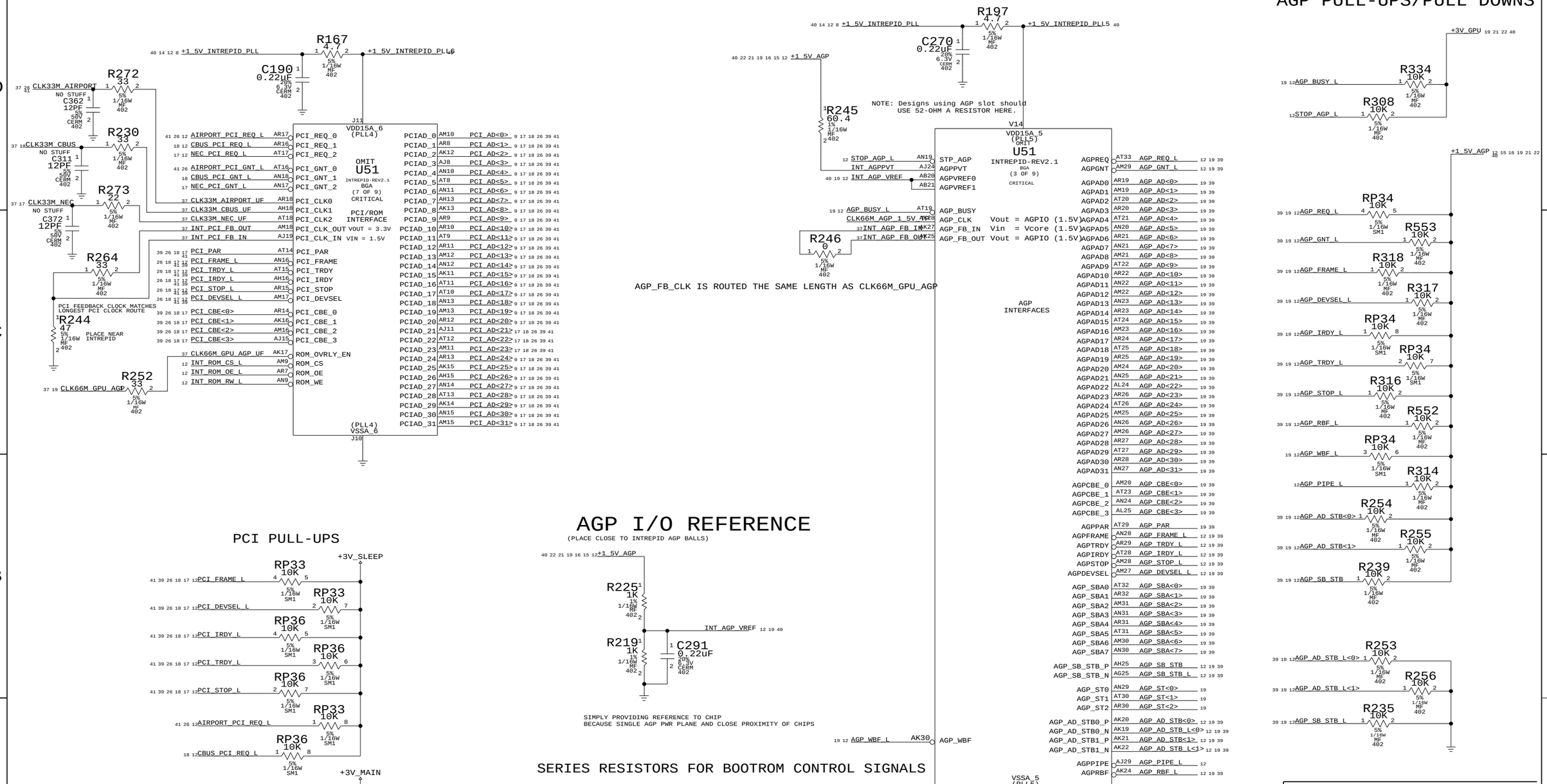
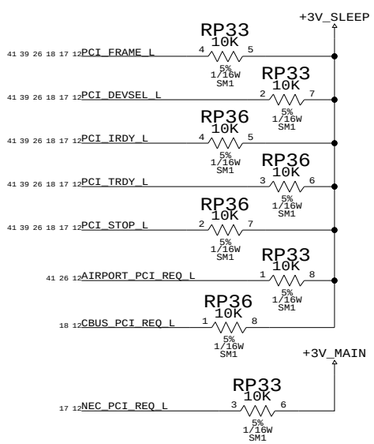
AGP PULL-UPS/PULL DOWNS



PCI PULL-UPS



NEC USB2 REQ REMAINS ON +3V_MAIN
BECAUSE THIS CHIP IS POWERED DURING SLEEP

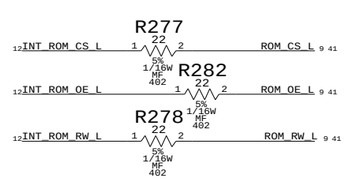
AGP I/O REFERENCE

(PLACE CLOSE TO INTREPID AGP BALLS)

SIMPLY PROVIDING REFERENCE TO CHIP
BECAUSE SINGLE AGP PWR PLANE AND CLOSE PROXIMITY OF CHIPS

SERIES RESISTORS FOR BOOTROM CONTROL SIGNALS

PLACE CLOSE TO INTREPID SIDE



INTREPID AGP/PCI

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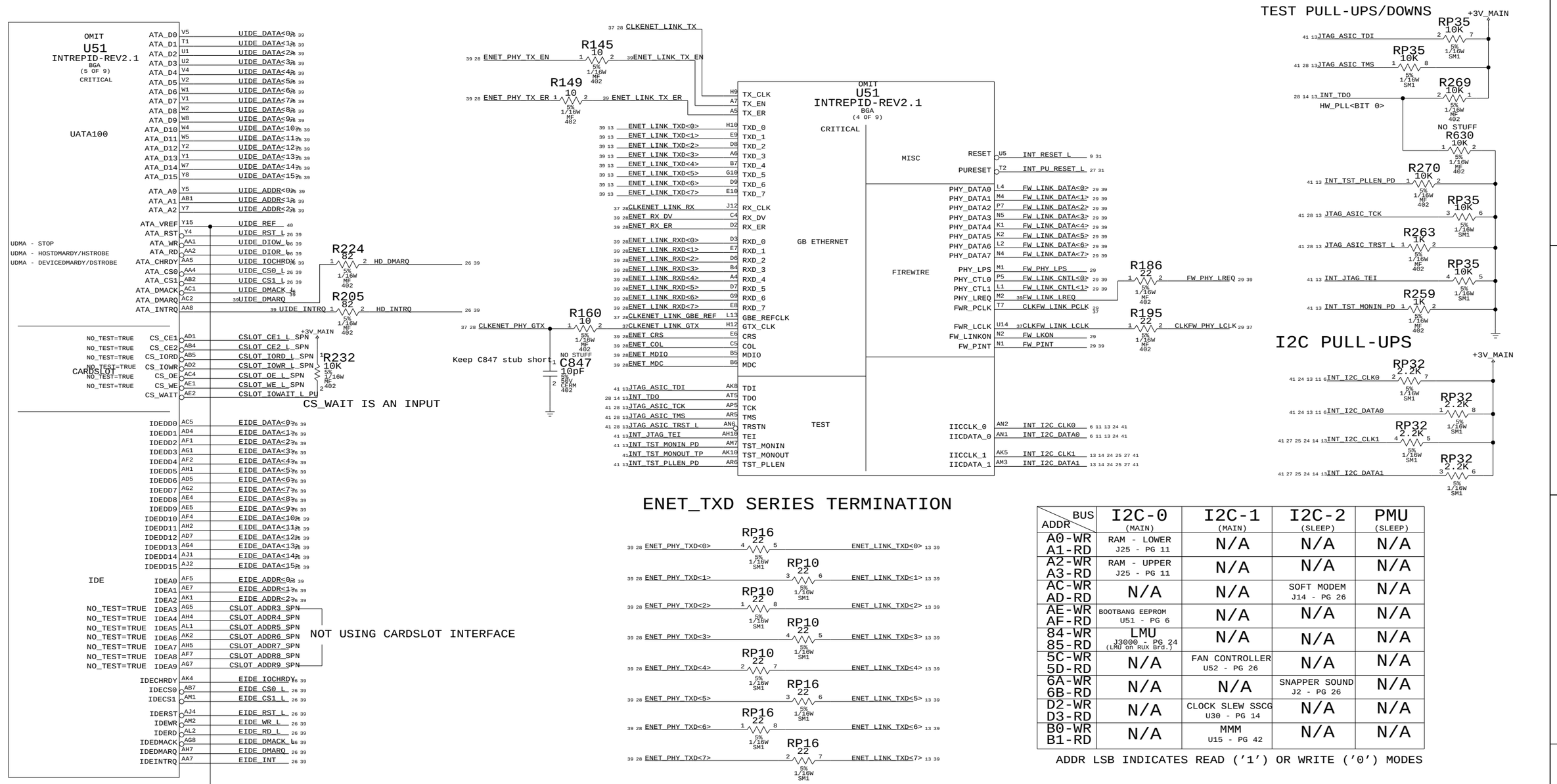

BUS / ADDR	I2C-0 (MAIN)	I2C-1 (MAIN)	I2C-2 (SLEEP)	PMU (SLEEP)
A0-WR A1-RD	RAM - LOWER J25 - PG 11	N/A	N/A	N/A
A2-WR A3-RD	RAM - UPPER J25 - PG 11	N/A	N/A	N/A
AC-WR AD-RD	N/A	N/A	SOFT MODEM J14 - PG 26	N/A
AE-WR AF-RD	BOOTBANG EEPROM U51 - PG 6	N/A	N/A	N/A
84-WR 85-RD	LMU J3000 - PG 24 (LMU on RUX Brd.)	N/A	N/A	N/A
5C-WR 5D-RD	N/A	FAN CONTROLLER U52 - PG 26	N/A	N/A
6A-WR 6B-RD	N/A	N/A	SNAPPER SOUND J2 - PG 26	N/A
D2-WR D3-RD	N/A	CLOCK SLEW SSCG U30 - PG 14	N/A	N/A
B0-WR B1-RD	N/A	MMM U15 - PG 42	N/A	N/A

ADDR LSB INDICATES READ ('1') OR WRITE ('0') MODES

JTG_RSTN_L	TST_TEI_H	JTG_TDO_H (I/O)	JTG_TDI_H (I/O)	TST_PLLEN_H	ANALYZER_CLK	DESCRIPTION
1	X	X	X	X	X	JTAG MODE
0	0	EXTPLL SHUTDOWN (OUTPUT)	DDR_ TPDENABLE (OUTPUT)	0	(OUTPUT)	NORMAL OPERATION
0	0	(OUTPUT)	0(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (SOFTWARE)
0	0	HWPLL_ TESTSEL5 (INPUT)	1(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (HARDWARE)
0	1	0(I)	0(I)	MEMWE	SYNC/MEM DATA BYPASS	ATPG NORMAL
0	1	0(I)	1(I)	0	X(I)	ATPG IDDQ
0	1	0(I)	1(I)	1	X(I)	TEST TRI-STATE
0	1	1(I)	0(I)	0	X(I)	FUNCTIONAL TEST WITHOUT POSTSCALAR BYPASS
0	1	1(I)	0(I)	1	X(I)	FUNCTIONAL TEST WITH POSTSCALAR BYPASS
0	1	1(I)	1(I)	X	X(I)	FUNCTIONAL TEST IDDQ

INT - ENET/FW/UATA EIDE/I2C

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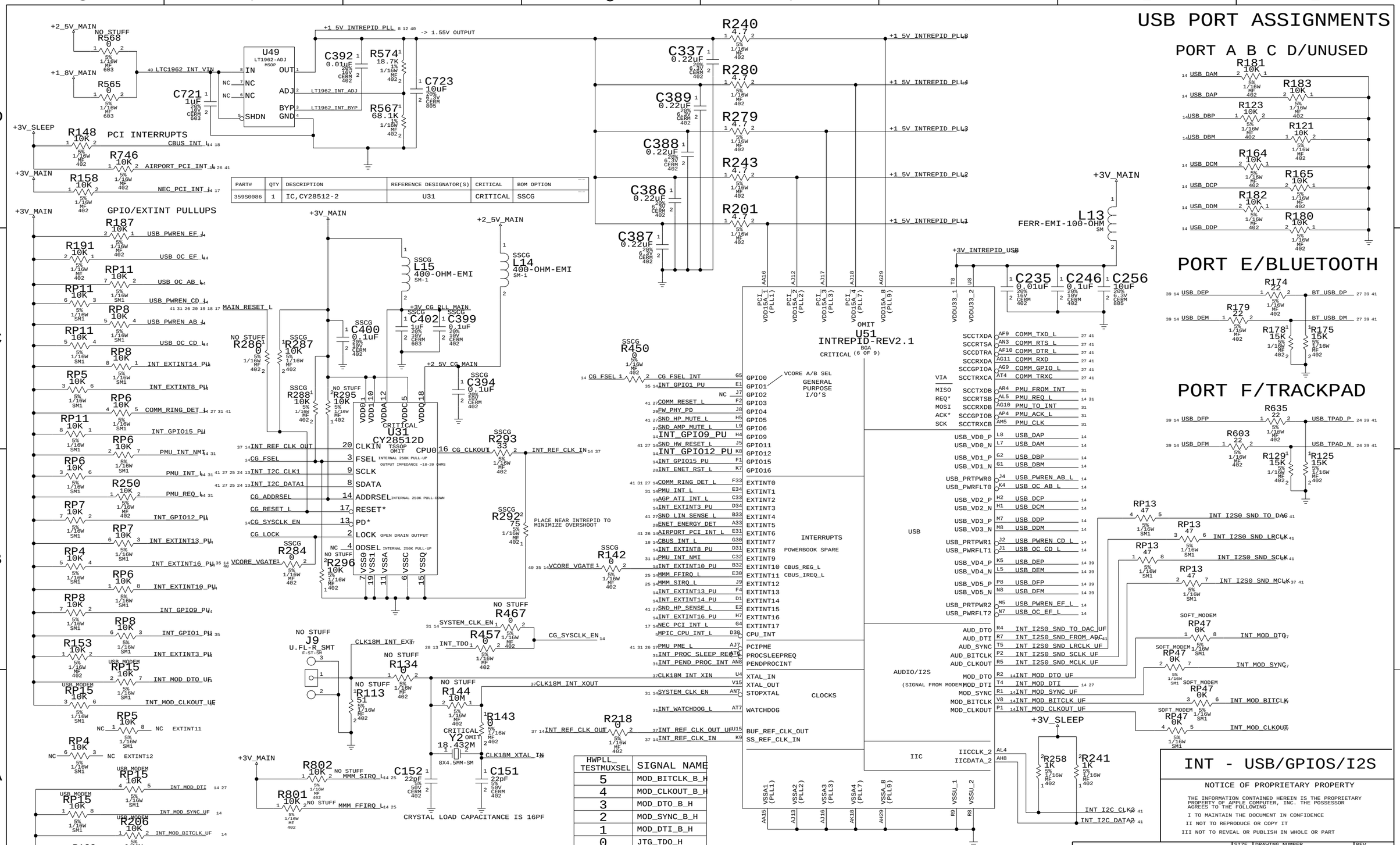
USB PORT ASSIGNMENTS

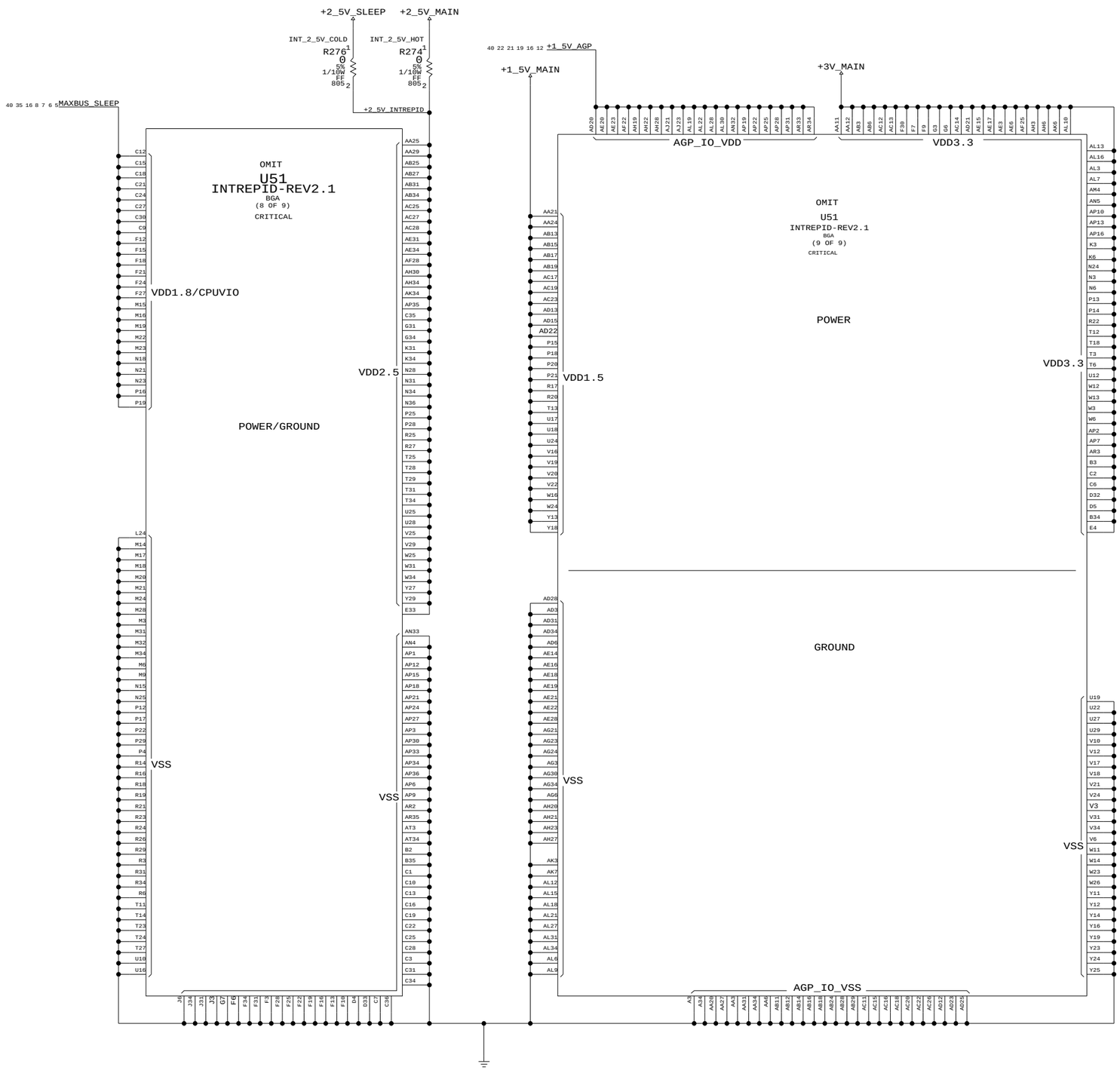


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
359S0086	1	IC,CY28512-2	U31	CRITICAL	SSCG

HWPLL_ TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0090	1	XTAL,CER,LOW PROF,18,432MHZ,8X4.5MM,SMD	Y2	CRITICAL	?

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES	RES-0402-V2	RESISTOR	10K		1/16W	5%	R292	NO_SSCG



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0305	1	IC,ASIC,INTREPID,REV2.1,974 BGA,FAST	U51	CRITICAL	?

Intrepid Power

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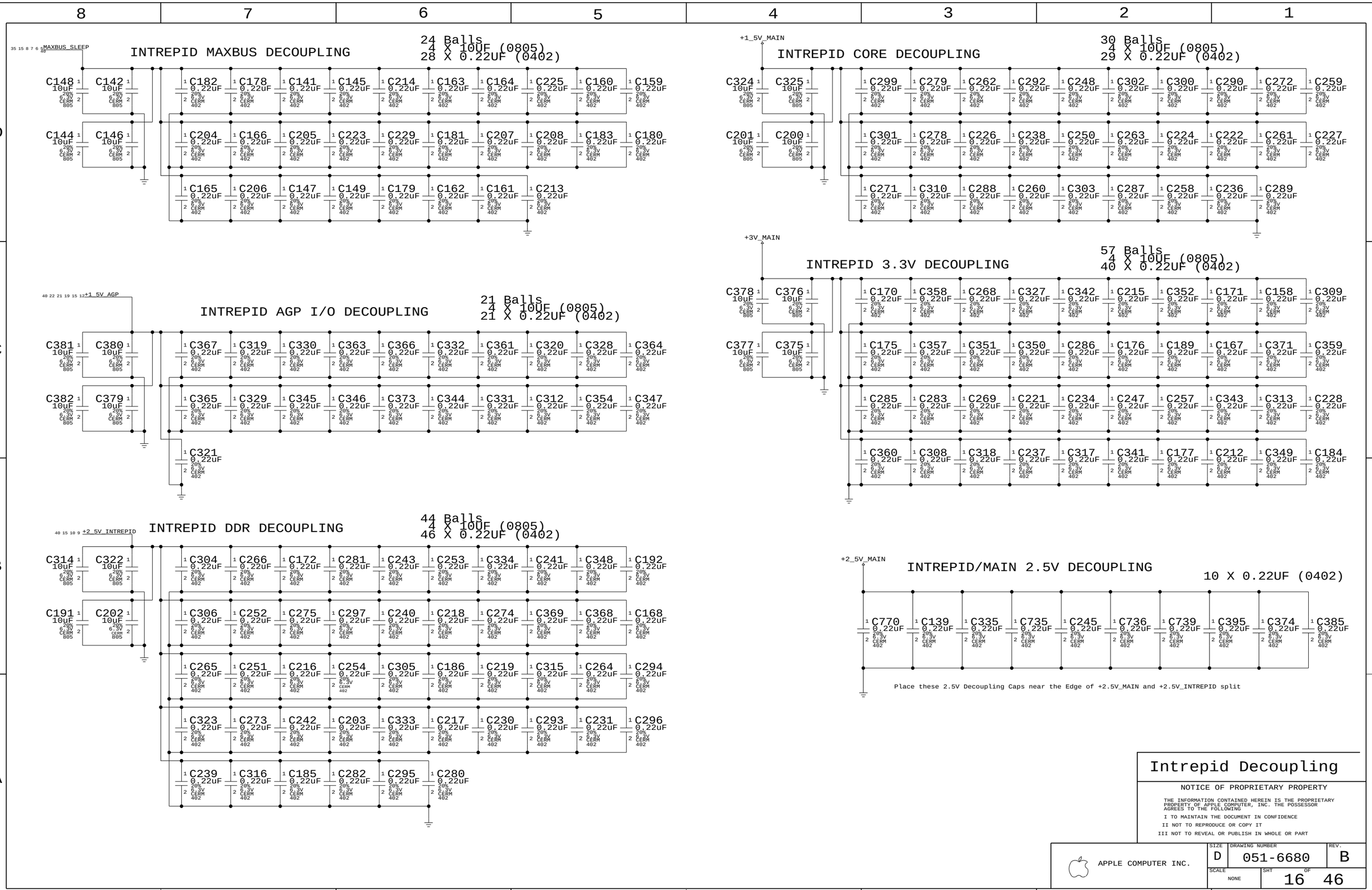

Intrepid Decoupling

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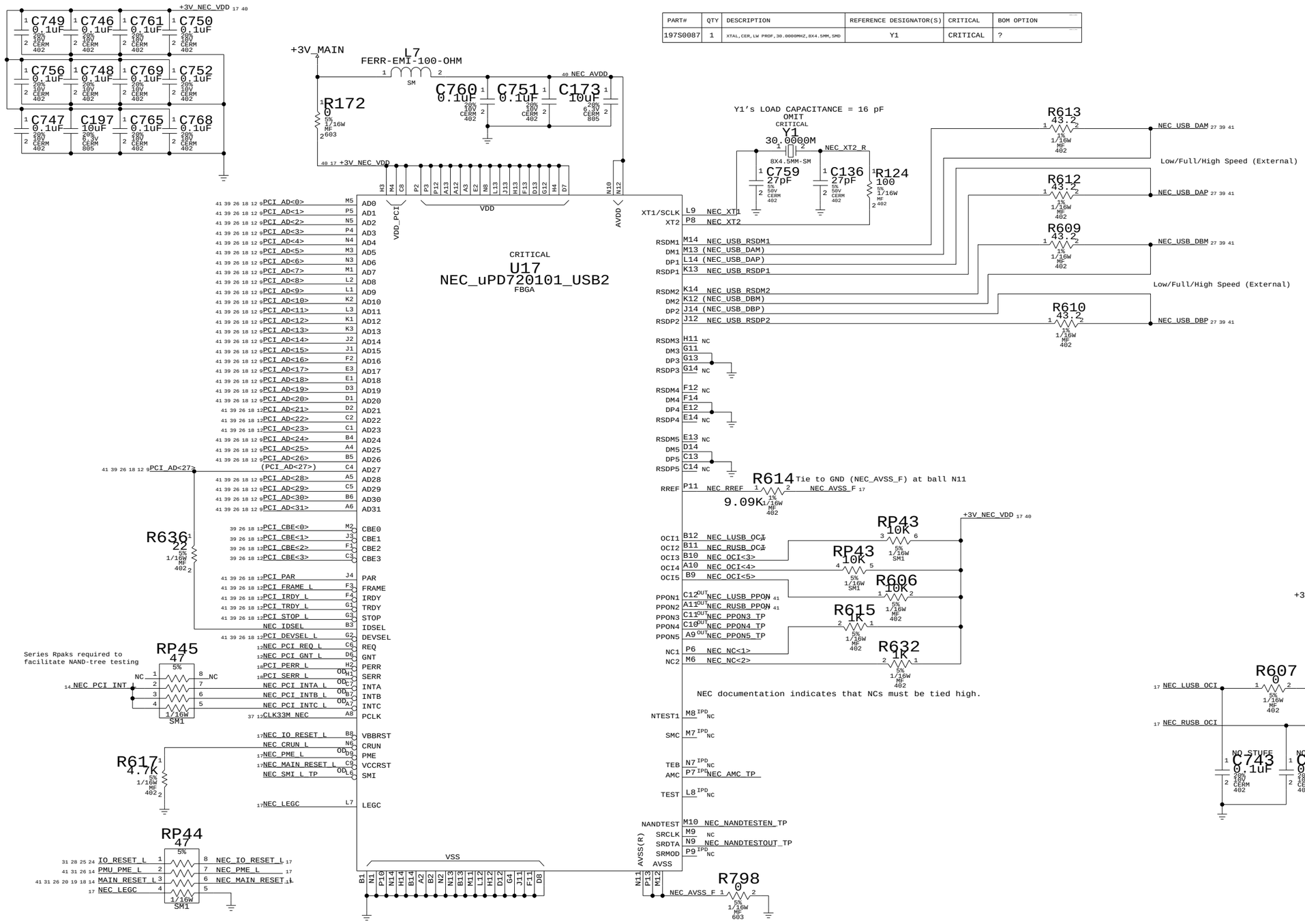
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0087	1	XTAL,CER,LW PROF,30.0000MHZ,8X4.5MM,SMD	Y1	CRITICAL	?



USB 2.0

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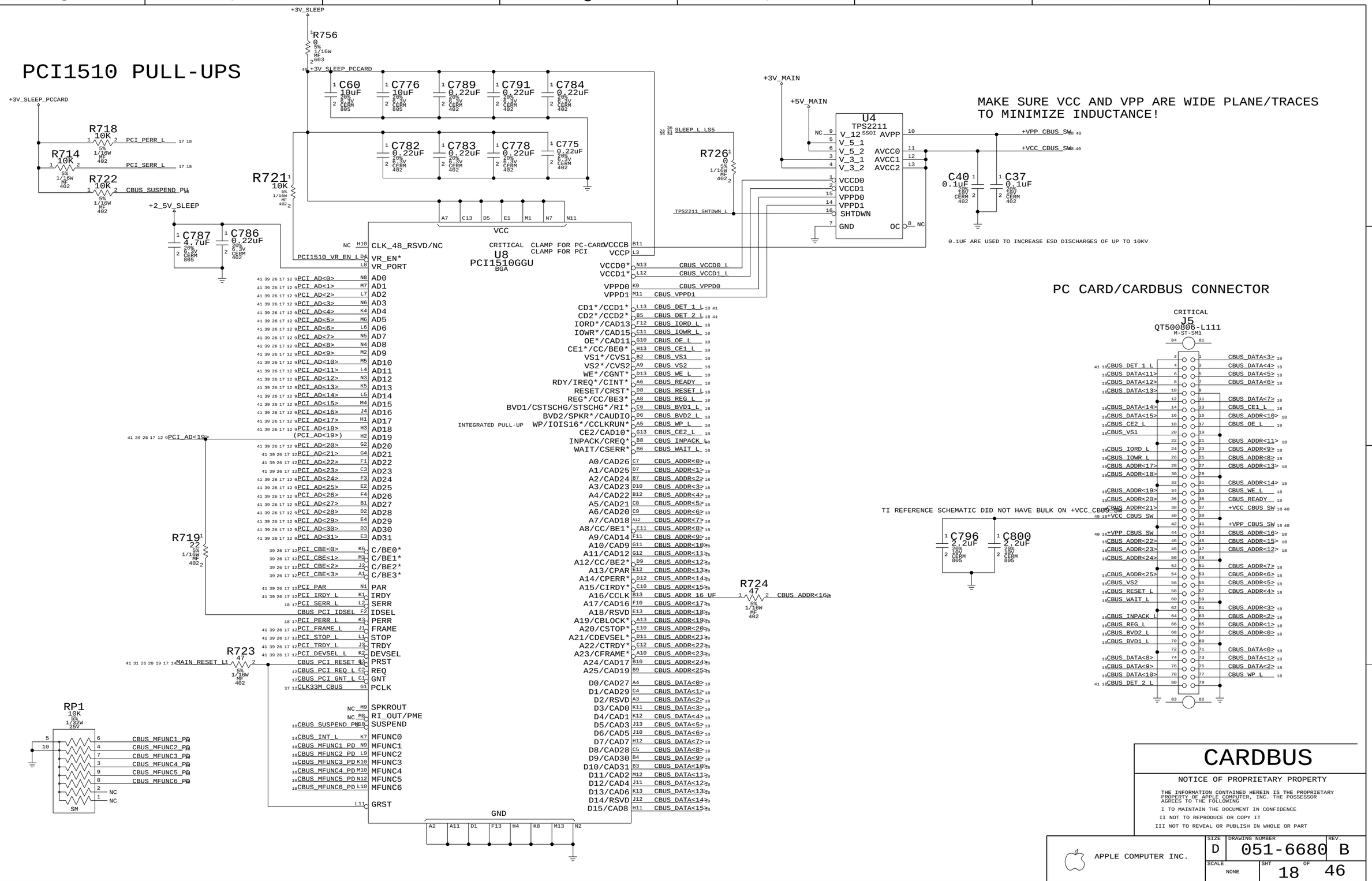
PCI1510 PULL-UPS



CARDBUS

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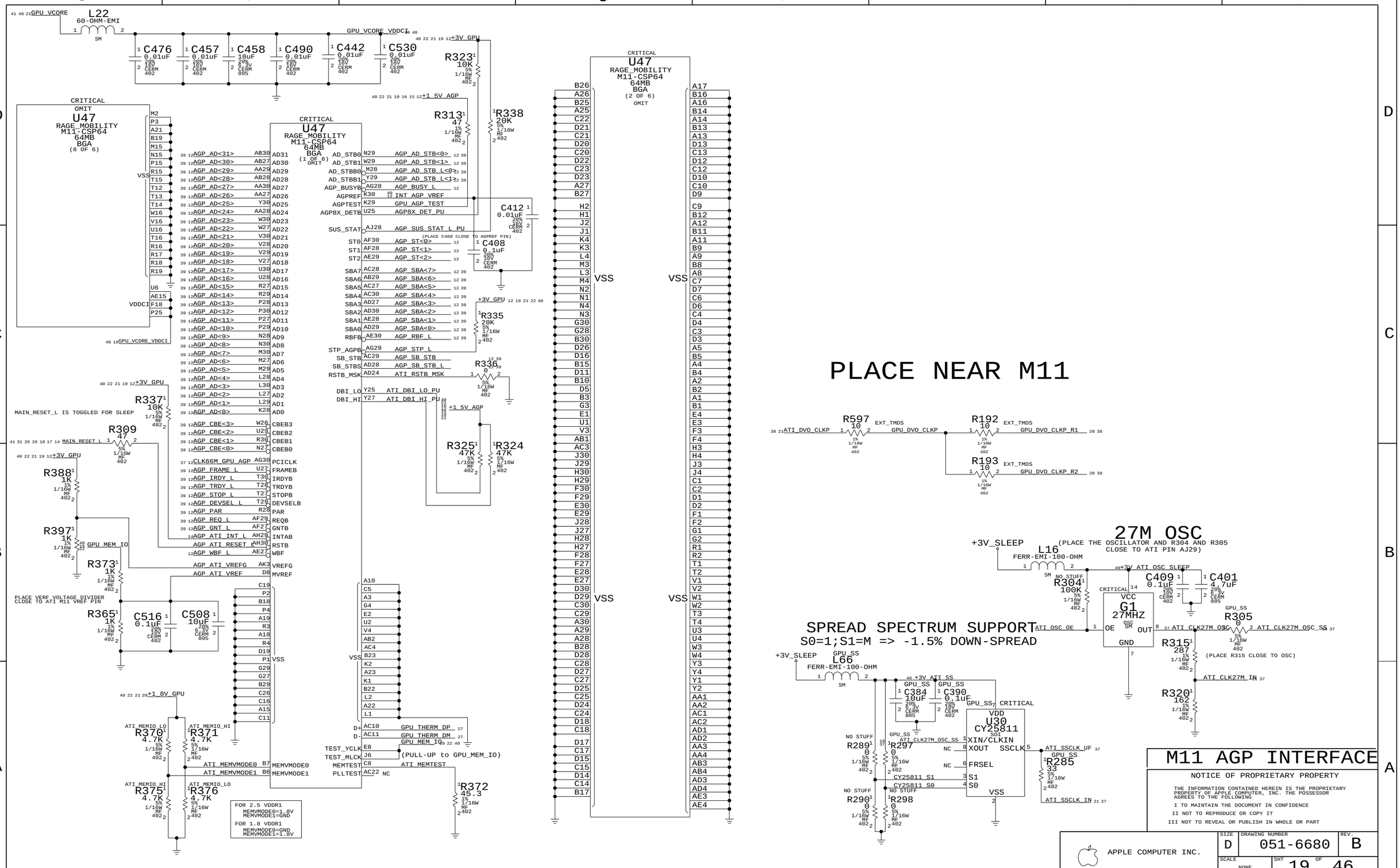
GPU_VCORE
L22
60-OHM-EMI
C476 0.01uF
C457 0.01uF
C458 10uF
C490 0.01uF
C442 0.01uF
C530 0.01uF
GPU_VCORE_VDDCI
+3V_GPU
R323 10K
+1_5V_AGP
R313 47
R338 20K
CRITICAL
OMIT
U47
RAGE_MOBILITY
M11-CSP64
64MB
BGA
(6 OF 6)
(1 OF 6)
(2 OF 6)
VSS
VDDCI
C412 0.01uF
C408 0.1uF
(PLACE C408 CLOSE TO AGPREF PIN)
R335 20K
R336 0
R337 10K
MAIN_RESET_L IS TOGGLED FOR SLEEP
R309 47
R325 47K
R324 47K
R388 1K
R397 1K
R373 1K
R365 1K
C516 0.1uF
C508 10uF
PLACE VERF VOLTAGE DIVIDER
CLOSE TO ATI M11 VREF PIN
+1_8V_GPU
R370 4.7K
R371 4.7K
R375 4.7K
R376 4.7K
R372 45.3
FOR 2.5 VDDR1
MEMVMODE0=1.8V
MEMVMODE1=GND
FOR 1.8 VDDR1
MEMVMODE0=GND
MEMVMODE1=1.8V
PLACE NEAR M11
R597 10
R192 10
R193 10
EXT_TMDS
ATI_DVO_CLKP
GPU_DVO_CLKP
GPU_DVO_CLKP_R1
GPU_DVO_CLKP_R2
27M OSC
+3V_SLEEP
L16
FERR-EMI-100-OHM
(PLACE THE OSCILLATOR AND R304 AND R305
CLOSE TO ATI PIN AJ29)
R304 100K
C409 0.1uF
C401 4.7uF
G1 27MHZ
VCC
OE
OUT
GND
R305 0
R315 287
(PLACE R315 CLOSE TO OSC)
R320 162
SPREAD SPECTRUM SUPPORT
S0=1;S1=M => -1.5% DOWN-SPREAD
L66
C384 10uF
C390 0.1uF
U30
CY25811
VDD
XIN/CLKIN
XOUT
FRSEL
S0
S1
SSCLK
R289 0
R297 0
R290 0
R298 0
R285 33
M11 AGP INTERFACE
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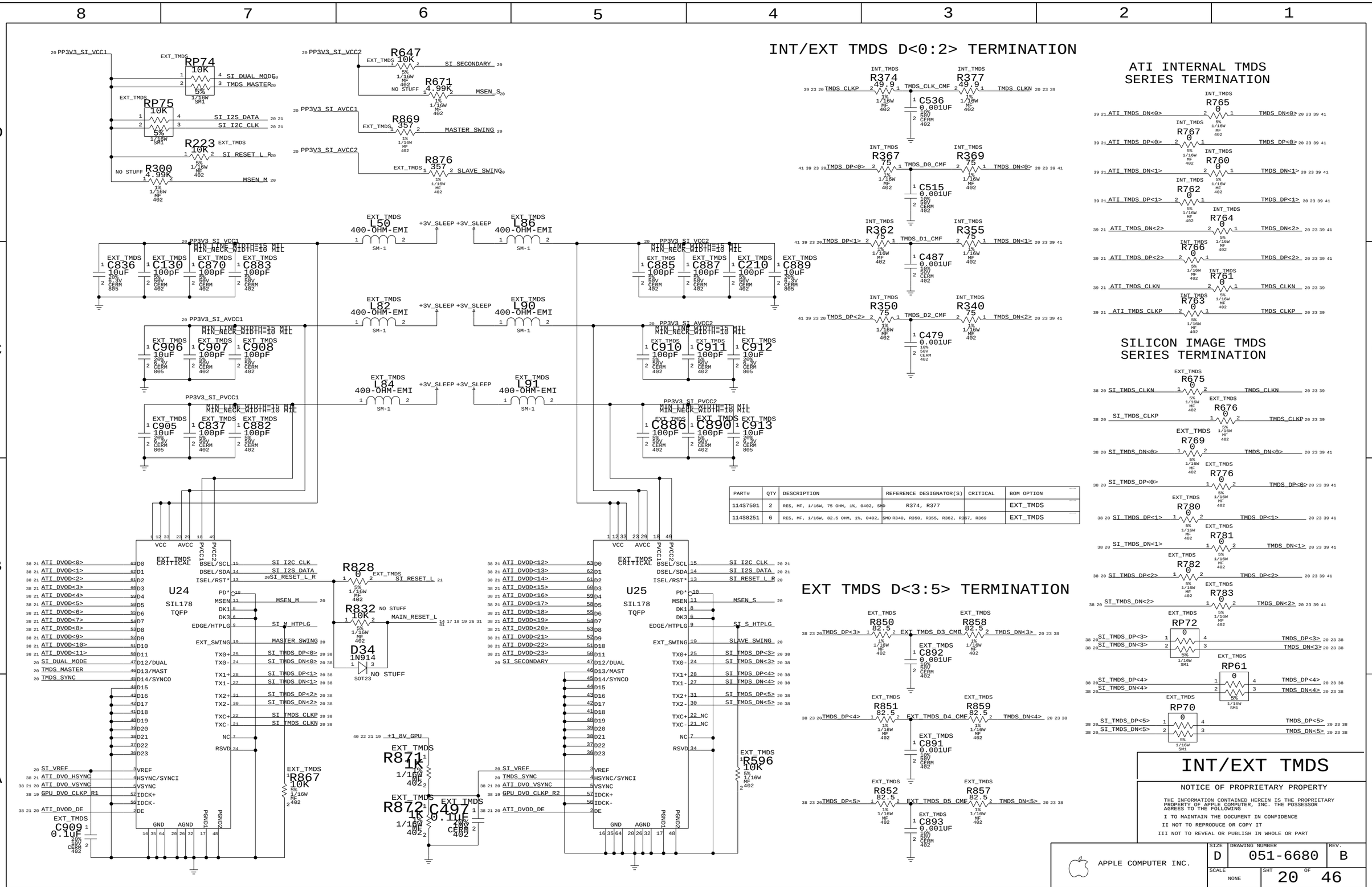
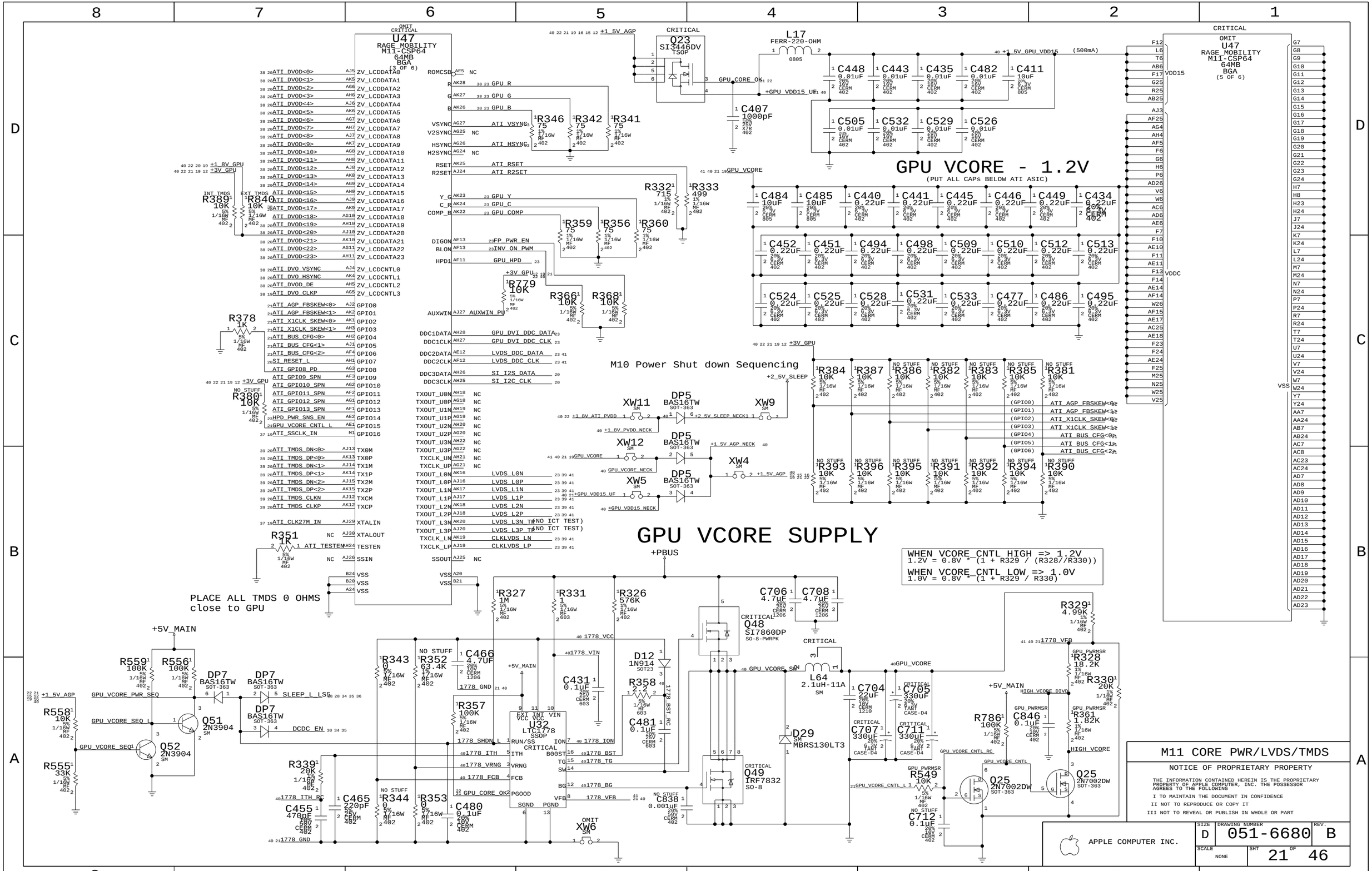


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S7501	2	RES, MF, 1/16W, 75 OHM, 1%, 0402, SMD	R374, R377		EXT_TMDS
114S8251	6	RES, MF, 1/16W, 82.5 OHM, 1%, 0402, SMD	R340, R350, R355, R362, R367, R369		EXT_TMDS


U47
RAGE_MOBILITY
M11-CSP64
64MB
BGA
(3 OF 6)
(5 OF 6)
Q23
SI3446DV
TSOP
L17
FERR-220-OHM
GPU VCORE - 1.2V
(PUT ALL CAPs BELOW ATI ASIC)
M10 Power Shut down Sequencing
GPU VCORE SUPPLY
WHEN VCORE_CNTL HIGH => 1.2V
1.2V = 0.8V * (1 + R329 / (R328//R330))
WHEN VCORE_CNTL LOW => 1.0V
1.0V = 0.8V * (1 + R329 / R330)
PLACE ALL TMDS 0 OHMS
close to GPU
U32
LTC1778
SSOP
Q48
SI7860DP
SO-8-PWRPK
Q49
IRF7832
SO-8
L64
2.1uH-11A
D29
MBRS130LT3
Q51
2N3904
Q52
2N3904
Q25
2N7002DW
SOT-363
M11 CORE PWR/LVDS/TMDS
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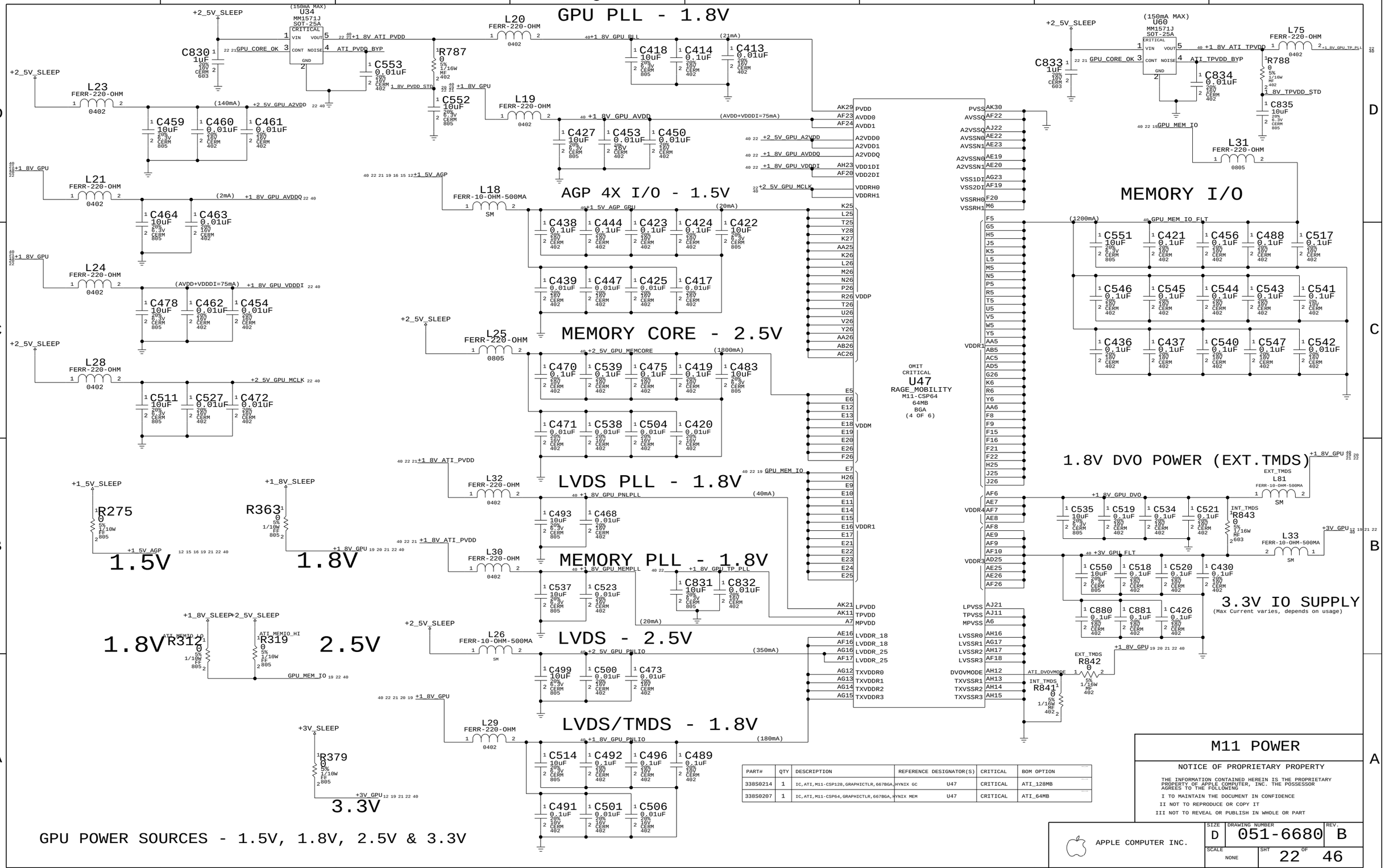

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0214	1	IC,ATI,M11-CSP128,GRAPHICTLR,667BGA,HYNIX GC	U47	CRITICAL	ATI_128MB
338S0207	1	IC,ATI,M11-CSP64,GRAPHICTLR,667BGA,HYNIX MEM	U47	CRITICAL	ATI_64MB

M11 POWER

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EXTERNAL VIDEO (DVI) INTERFACE

VGA SYNC BUFFERS

+3V_MAIN
74AHC1G32 U40 SM
ATI_VSYNC → ATI_VSYNC_BUF
OMIT L38 FERR-60-OHM-0.1A 0402 → VGA_VSYNC

PLACE L1002 & L1003 CLOSE TO DVI CONNECTOR

+3V_MAIN
74AHC1G32 U39 SM
ATI_HSYNC → ATI_HSYNC_BUF
OMIT L36 FERR-60-OHM-0.1A 0402 → VGA_HSYNC

TMDS FILTERING
PLACE CLOSE TO CONNECTOR

L37 370-OHM SM
TMDS_CLKP, TMDS_CLKN → TMDS_CONN_CLKP, TMDS_CONN_CLKN

ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

FL1 LCFILTER SM-220MHZ CRITICAL — GPU_B → VGA_B
FL2 LCFILTER SM-220MHZ CRITICAL — GPU_G → VGA_G
FL3 LCFILTER SM-220MHZ CRITICAL — GPU_R → VGA_R

C641 3.3pF 0.25% 50V CERM 402
R462 75 1% 1/16W MF 402 NO STUFF
C634 3.3pF 0.25% 50V CERM 402
R458 75 1% 1/16W MF 402 NO STUFF
C631 3.3pF 0.25% 50V CERM 402
R456 75 1% 1/16W MF 402 NO STUFF

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)

+5V_SLEEP F2 CRITICAL 0.5AMP-13.2V SM → +5V_DDC_SLEEP_UF
L42 400-OHM-EMI SM-1 → +5V_DDC_SLEEP

CRITICAL J22 QH1112 F-RT-TH

CRITICAL L45 90-OHM-300mA 2012H
TMDS_DN<0>, TMDS_DP<0> → TMDS_CONN_DN<0>, TMDS_CONN_DP<0>

TMDS_CONN_DN<5>, TMDS_DP<5>, TMDS_CONN_CLKP, TMDS_CONN_CLKN, VGA_B, VGA_HSYNC
TMDS_CONN_DN<2>, TMDS_CONN_DN<1>, TMDS_CONN_DP<2>, TMDS_CONN_DP<1>, TMDS_CONN_DN<4>, TMDS_CONN_DN<3>, TMDS_CONN_DP<4>, TMDS_CONN_DP<3>
DVI_DDC_CLK_UF, (+5V_DDC_SLEEP), DVI_DDC_DATA_UF, VGA_VSYNC, DVI_HPD_UF, VGA_R, VGA_G

C667 0.01uF 20% 50V CERM 603
PLACE NEAR C5A & C5B
R464 0 5% 1/16W MF 402
R463 0 5% 1/16W MF 402
PLACE NEAR 3, 11 & 19

Isolation required for DVI power switch
D19 SM MBR0530
DDC_CLK_ISO
R478 4.7K 5% 1/16W MF 402
R476 4.7K 5% 1/16W MF 402
R479 100 5% 1/16W MF 402
C654 100pF 5% 25V CERM 201
C655 100pF 5% 25V CERM 201
C653 100pF 5% 25V CERM 201

3V LEVEL SHIFTERS
+3V_SLEEP

Q39 2N7002DW SOT-363 — DVI_DDC_CLK
Q39 2N7002DW SOT-363 — DVI_DDC_DATA
Q40 2N7002DW SOT-363 — DVI_HPD
R480 10K 5% 1/16W MF 402 → GPU_DVI_DDC_CLK
R474 10K 5% 1/16W MF 402 → GPU_DVI_DDC_DATA
R481 100K 5% 1/16W MF 402 → GPU_HPD

NOTE: Pulldown for DVI_HPD provided by DVI power switch interface

CRITICAL L47 90-OHM-300mA 2012H
TMDS_CONN_DN<2>, TMDS_CONN_DP<2>
CRITICAL L46 90-OHM-300mA 2012H
TMDS_CONN_DN<1>, TMDS_CONN_DP<1>
CRITICAL L44 90-OHM-300mA 2012H EXT_TMDS
TMDS_DN<3>, TMDS_DP<3> → TMDS_CONN_DN<3>, TMDS_CONN_DP<3>

DVI POWER SWITCH

Power key detect path when system is shutdown or asleep.. DDC CLK is isolated from NV17M DURING SHUTDOWN. WHEN power key on remote device is pressed, 5V will be driven into DDC CLK. Since host rails will be low, TP0610 will turn on, driving SOFT_PWR_ON low. As host rails rise, TP0610 will turn off, so pull remote device back to DDC CLK. Isolation will be disabled as well.

Q38 TP0610 SM
DVI_DDC_CLK_UF, DVI_TURN_ON, +5V_DDC_SLEEP
R473 680 5% 1/16W MF 402
DVI_TURN_ON_BLOCK, DVI_TURN_ON_LIM
R460 10K 5% 1/16W MF 402
Q35 MMDT3904 SOT-363 — SOFT_PWR_ON_L
R459 330 5% 1/16W MF 402
Pulldown prevents 3904 from turning on when DVI monitor has active, self-powered DDC clock pullup.

+3V_SLEEP
Power key detect path when system is running. HPD normally driven to 3.3V. When power key on remote device pressed, HPD will be driven to 5V. COMPARATOR ENABLED BY NV17MAP
R485 68.1K 1% 1/16W MF 402
C668 0.1uF 20% 10V CERM 402
HPD_4V_REF
U42 LMC7211 SM
R472 10K 1% 1/16W MF 402 — DVI_HPD_UF → DVI_HPD_DIV
R475 10K 1% 1/16W MF 402 — HPD_PWR_SW_BASE → Q35 MMDT3904 SOT-363
R482 10K 1% 1/16W MF 402
R484 100K 1% 1/16W MF 402
HPD_PWR_SW
R470 330 5% 1/16W MF 402
HPD_REF_EN_L
Q40 2N7002DW SOT-363
HPD_PWR_SNS_EN
R483 470K 5% 1/16W MF 402

CRITICAL L49 90-OHM-300mA 2012H EXT_TMDS
TMDS_DN<4>, TMDS_DP<4> → TMDS_CONN_DN<4>, TMDS_CONN_DP<4>
CRITICAL L85 90-OHM-300mA 2012H EXT_TMDS
TMDS_DN<5>, TMDS_DP<5> → TMDS_CONN_DN<5>, TMDS_CONN_DP<5>

LCD INTERFACE
LVDS INTERFACE

+3V_MAIN
LCD POWER SWITCH
R347 100K 5% 1/16W MF 402
C474 2200pF 5% 50V CERM 603
R354 100K 5% 1/16W MF 402 — LCD_PWREN_L
LCD_DIGON_L
Q29 SI3443DV TSOP
+3V_LCD_SW
L27 FERR-250-OHM SM → +3V_LCD (LVDS DDC POWER)
C503 0.001uF 20% 50V CERM 402
Q28 2N7002 SM — FP_PWR_EN
+3V_SLEEP
R543 100K 5% 1/16W MF 402
R544 100K 5% 1/16W MF 402
C701 0.001uF 20% 50V CERM 402
LVDS_DDC_CLK, LVDS_DDC_DATA
100K pull-ups are for no-panel case (development) Panel has 2K pull-ups
NO STUFF C702 0.001uF 20% 50V CERM 402
C548 0.001uF 20% 50V CERM 402
C549 0.001uF 20% 50V CERM 402

CRITICAL J14 G-501973 F-RT-SM
LVDS_DDC_CLK, LVDS_DDC_DATA, LVDS_L0N, LVDS_L0P, LVDS_L1N, LVDS_L1P, LVDS_L2N, LVDS_L2P, CLKLVDS_LN, CLKLVDS_LP

INVERTER INTERFACE

+PBUS
L73 FERR-1K-OHM-EMI SM → +14V_INV
+5V_MAIN
Q76 FDG6324L SC70-6
+5V_INV_UF_SW
L74 400-OHM-EMI SM-1 → +5V_INV_SW
R750 100K 5% 1/16W MF 402 — FP_PWR_EN_L
C813 10uF 20% 6.3V CERM 805
C812 0.001uF 20% 50V CERM 402
CRITICAL J4 SM-2MT
Q76 FDG6324L SC70-6 — FP_PWR_EN
L72 400-OHM-EMI SM-1 → BRIGHT_PWM
C815 0.001uF 20% 50V CERM 402
+3V_MAIN
C816 0.001uF 20% 50V CERM 402
C19 0.001uF 20% 50V CERM 402
INV_GND
L1 FERR-250-OHM SM
C22 0.1uF 20% 10V CERM 402
INV_ON_PWM
U2 NC7S32 SC70
BRIGHT_PWM_UF
INVERTER EXPECTS ACTIVE HIGH SIGNAL

R753 0 5% 1/16W MF 402
C819 0.01uF 20% 25V CERM 603

S-VIDEO/COMP OUT INTERFACE

Place GND shorts at graphics controller
XW15 SM
L54 FERR-10-OHM-500MA SM — GPU_TV_GND1 → TV_GND1
C657 0.01uF 20% 50V CERM 603
L53 3.3uH 0603 — GPU_Y
C663 560pF 10% 50V CERM 402
C656 560pF 10% 50V CERM 402
L57 3.3uH 0603 — GPU_C
C661 560pF 10% 50V CERM 402
C660 560pF 10% 50V CERM 402
L55 3.3uH 0603 — GPU_COMP
C664 560pF 10% 50V CERM 402
C658 560pF 10% 50V CERM 402
XW14 SM
L56 FERR-10-OHM-500MA SM — GPU_TV_GND2 → TV_GND2
C659 0.01uF 20% 50V CERM 603
Place GND shorts at graphics controller

CRITICAL J21 MINIDIN RT-TH MH11773-WMR8A
TV_C, TV_Y, TV_COMP

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S1331	2	DISCRETE,RES,33OHM,0402	L36,L38		VGA_BUFFER_RES

VIDEO CONNECTORS

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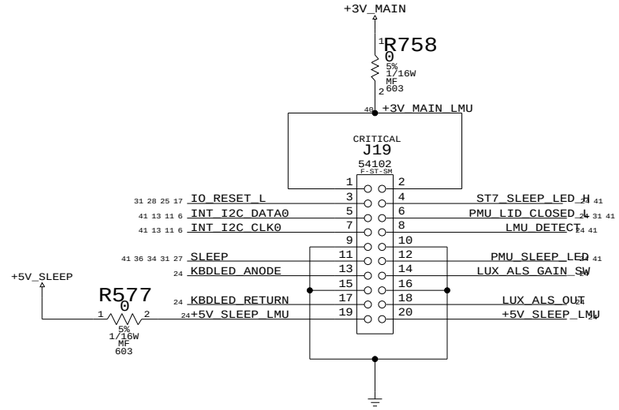
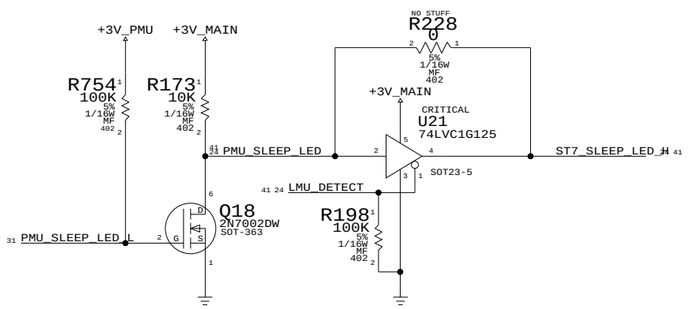
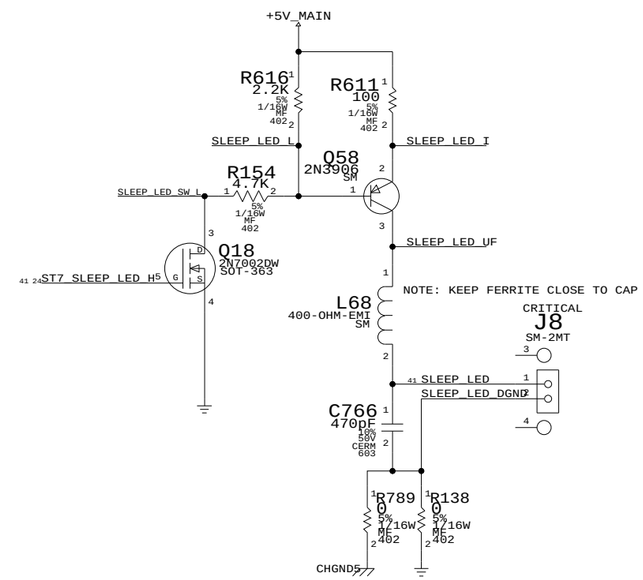
LMU/RIGHT SENSOR CONNECTOR

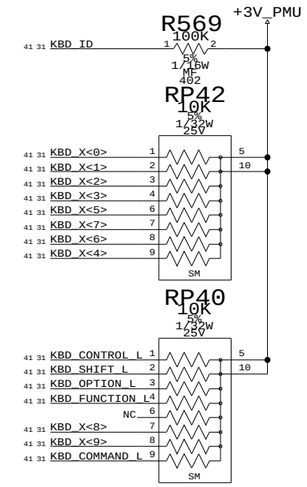




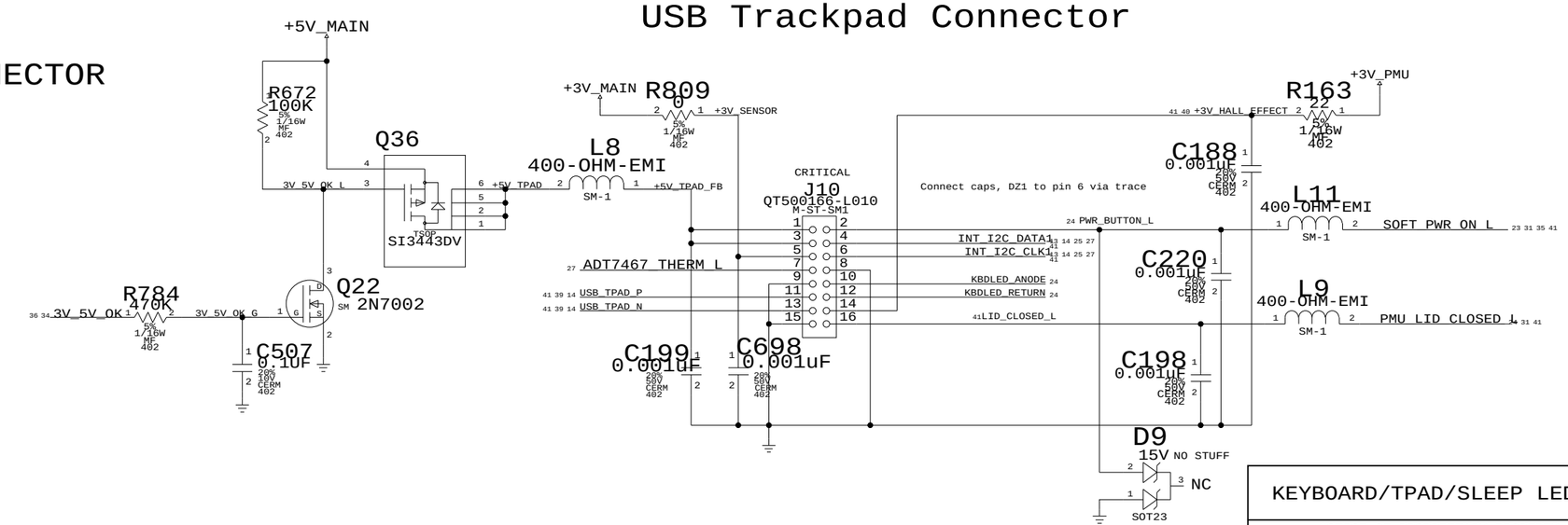
SLEEP LED



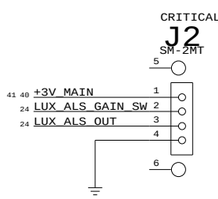
KEYBOARD PULLUPS



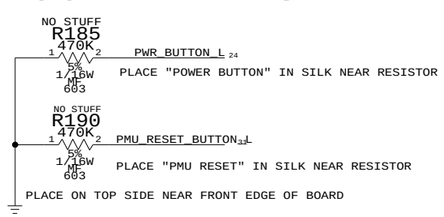
USB Trackpad Connector



LEFT LIGHT SENSOR CONNECTOR



DEBUG HELPERS



KEYBOARD/TPAD/SLEEP LED

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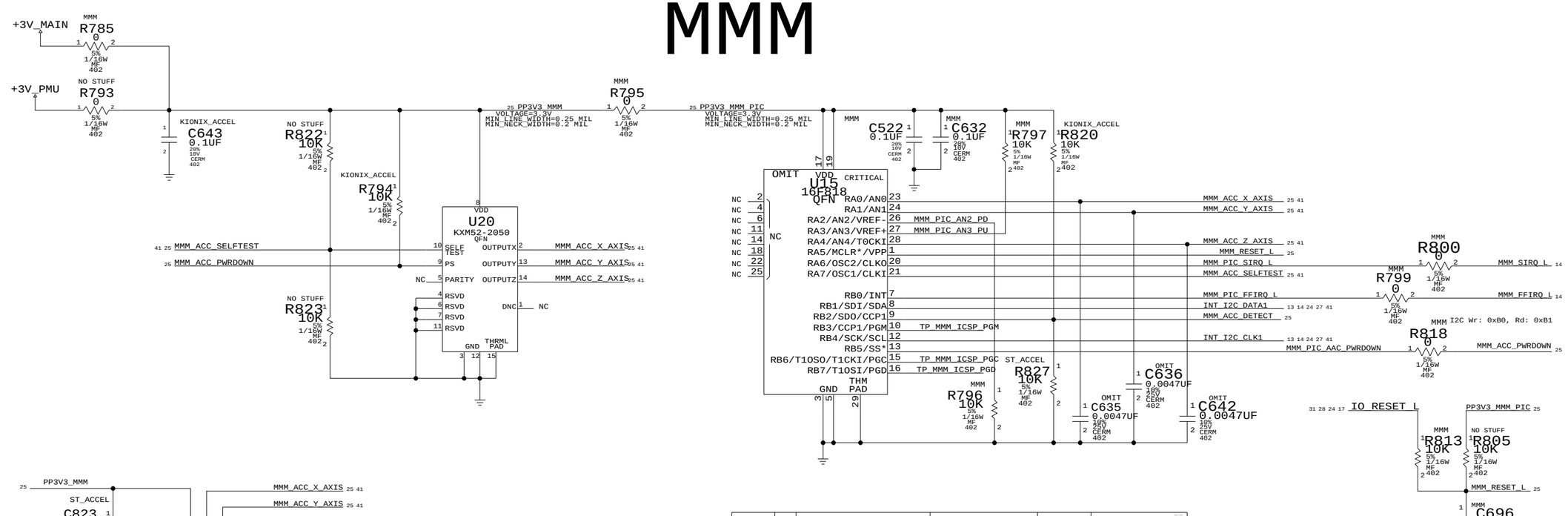
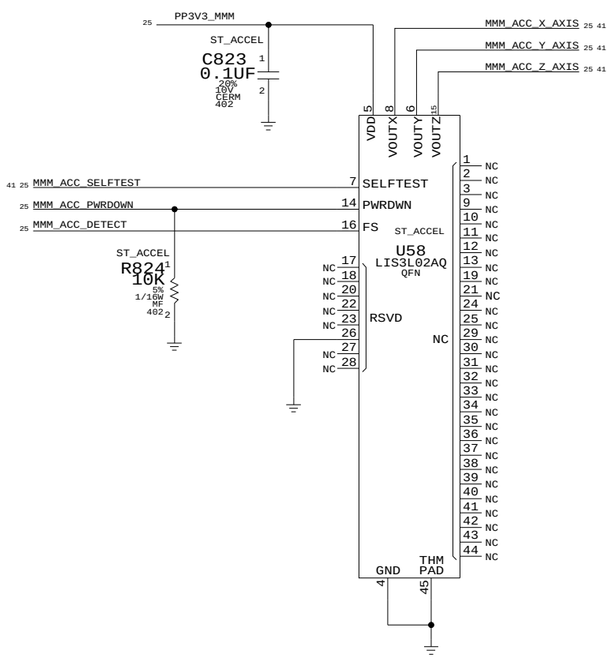
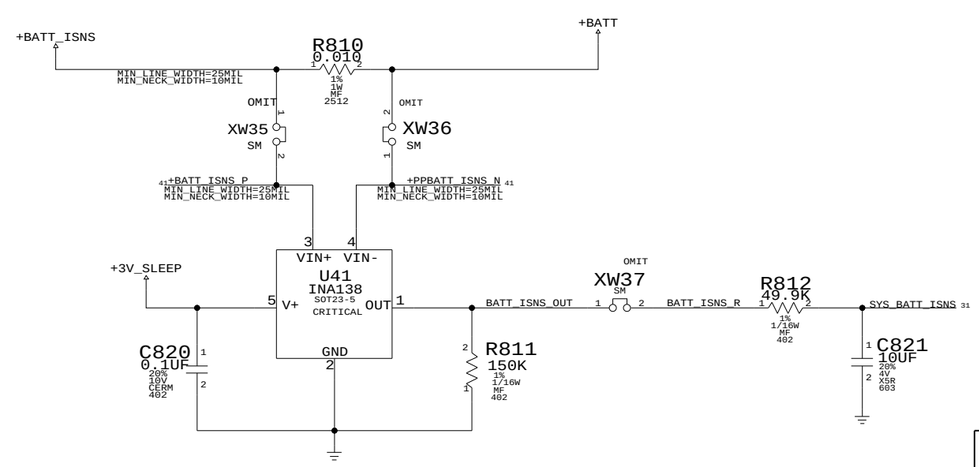
MMM



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0131	3	CAP CER.033UF,10%,16V,X7R/X5R,0402,SMD	C635,C636,C642		KIONIX_ACCEL
132S0072	3	CAP CER .0015UF, 10%, 25V, X7R, 0402, SM	C635,C636,C642		ST_ACCEL
341S1630	1	IC,UCTLR,MMM,PIC16F818,SMD, W/PROGRAM	U15	CRITICAL	MMM



BATTERY CURRENT SENSE



MMM & BATTERY CURRENT SENSOR

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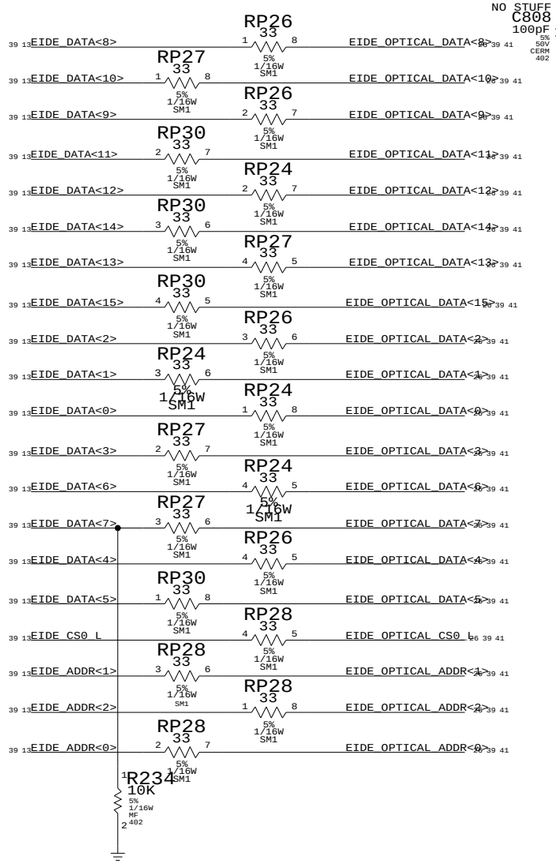
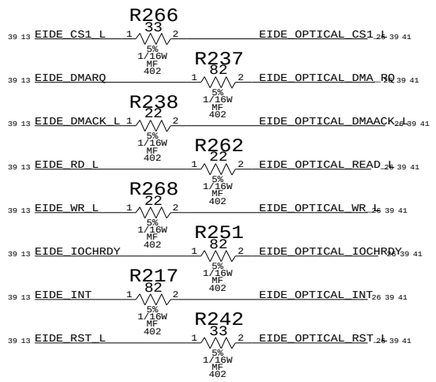
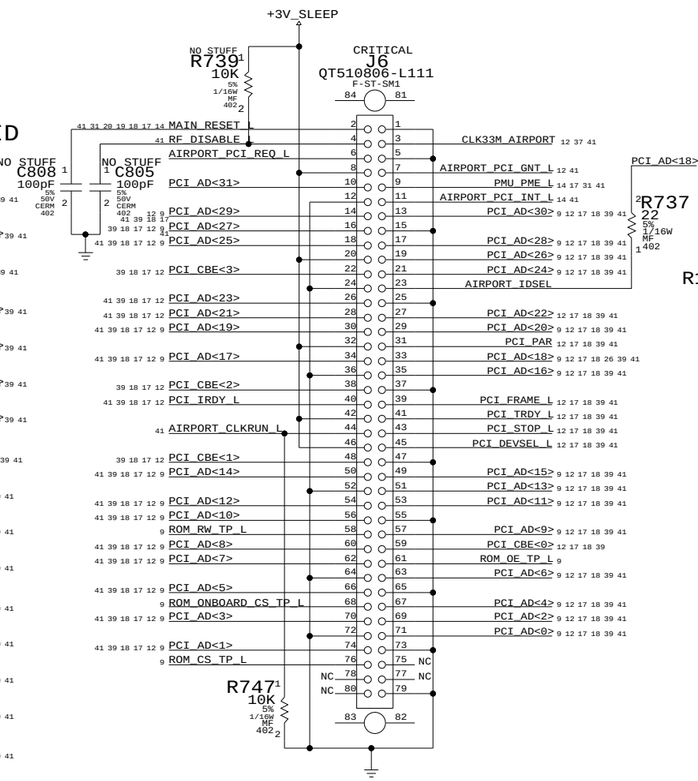
WIRELESS INTERFACE

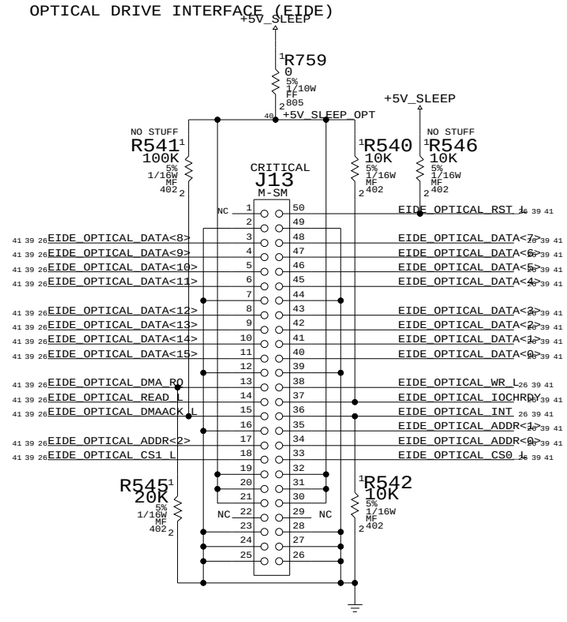
EIDE SERIES TERMINATION
PLACE TERMINATORS NEAR INTREPID





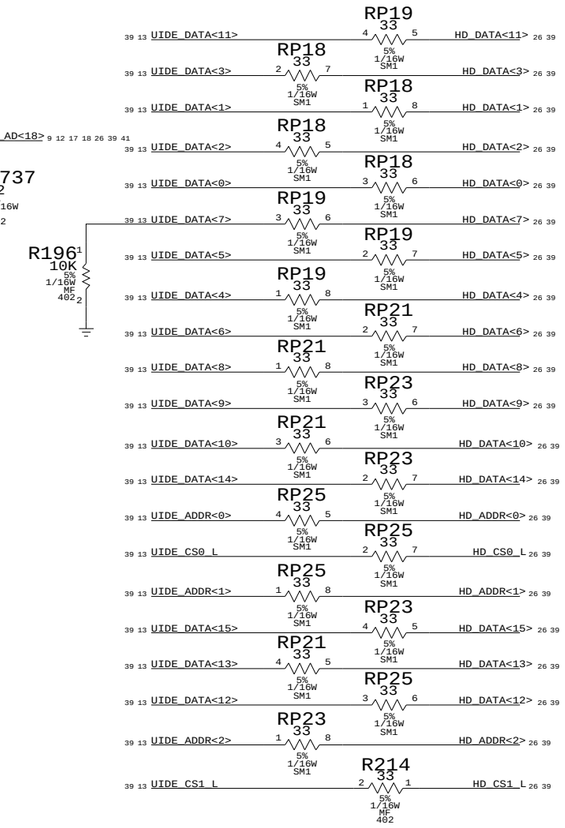


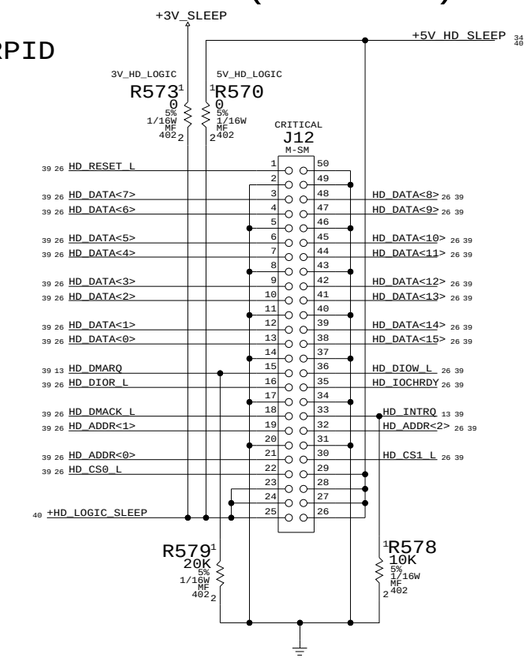
OPTICAL DRIVE INTERFACE (EIDE)



HARD DRIVE INTERFACE (UATA100)

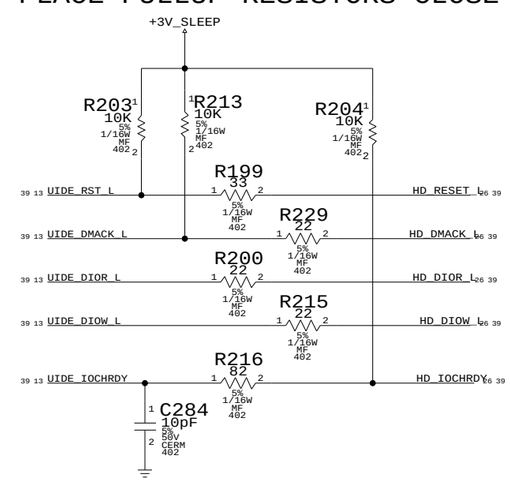
PLACE SERIES R CLOSE TO INTERPID





ANY SEQUENCING REQUIREMENT BETWEEN +5V_HD_SLEEP AND +3V_SLEEP

PLACE PULLUP RESISTORS CLOSE TO INTREPID



IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V

INTERNAL I/O CONNECTORS

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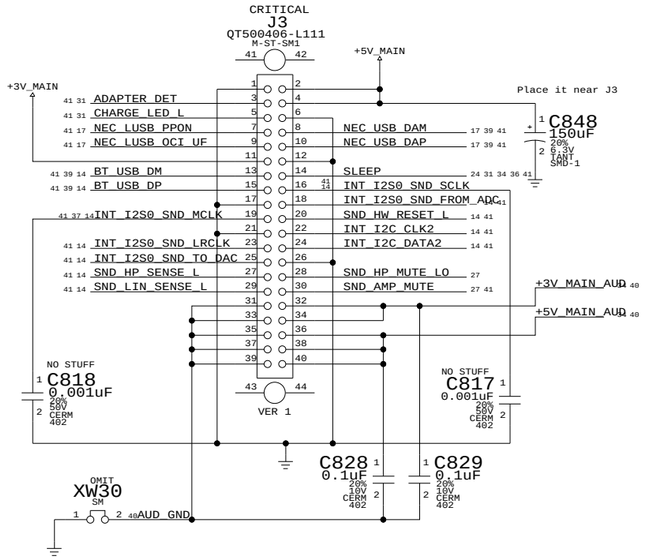
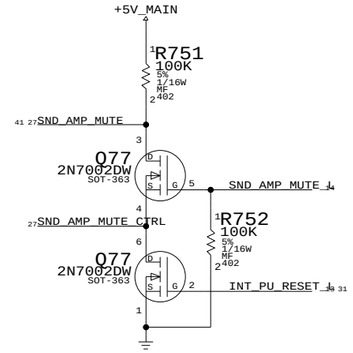
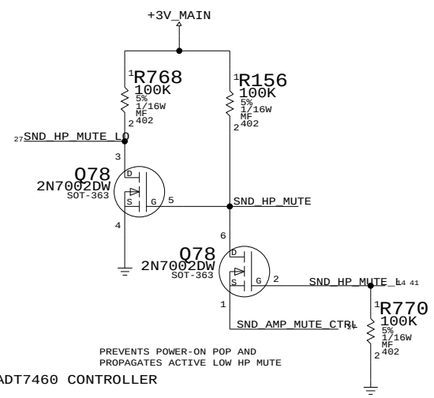
LEFT I/O & AUDIO BOARD (LIO)



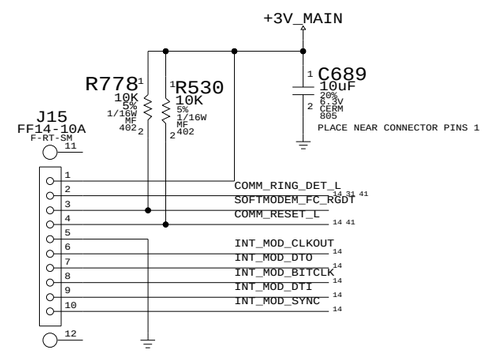


PREVENTS POWER-ON POP AND
GENERATES ACTIVE HIGH SPKR MUTE

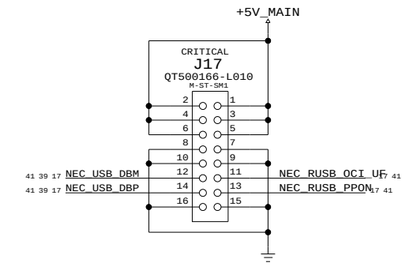


PREVENTS POWER-ON POP AND
PROPAGATES ACTIVE LOW HP MUTE

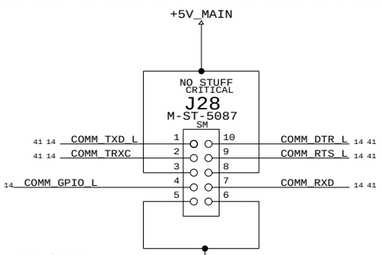
SOFT MODEM CONN



RIGHT USB BOARD



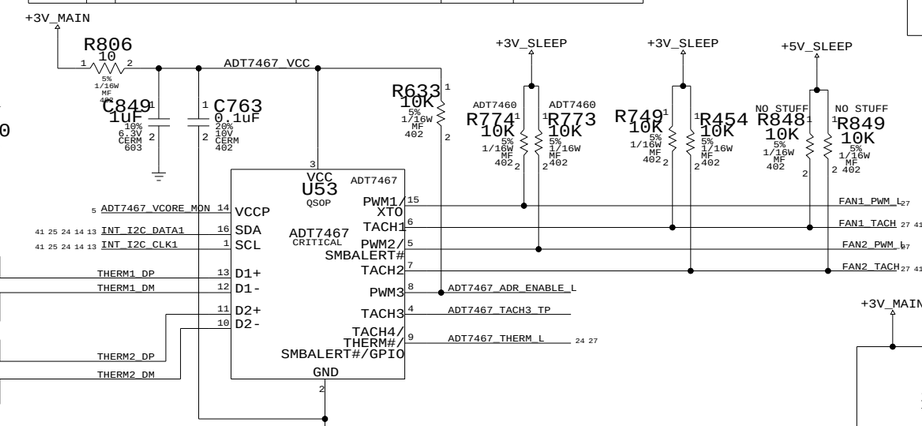
SERIAL DEBUG INTERFACE



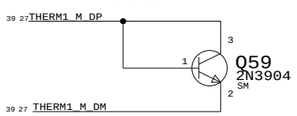
FAN INTERFACE

FAN CONTROLLER

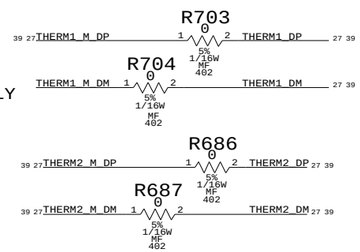
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S0608	1	IC,ADT7460,FAN CTLR,16P QSOP	U53	CRITICAL	ADT7460



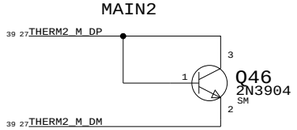
PLACE CLOSE TO CPU
MAIN1



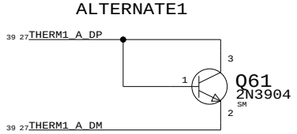
KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER



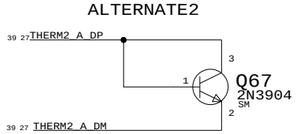
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY
MAIN2



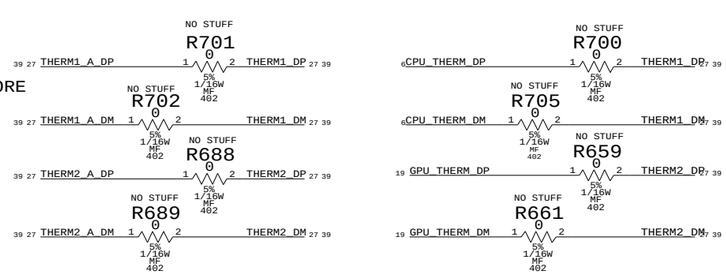
PLACE UNDERNEATH UPPER RAM
ALTERNATE1



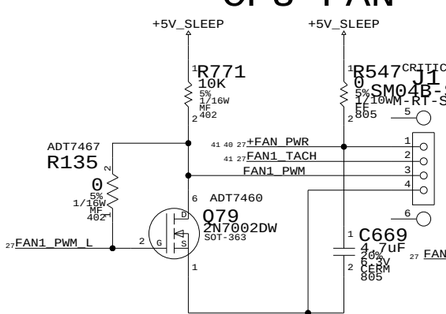
PLACE CLOSE TO BATTERY CHARGER/VCORE
ALTERNATE2



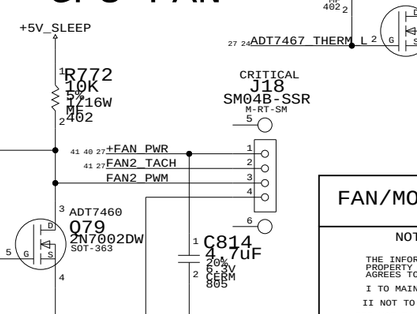
KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER

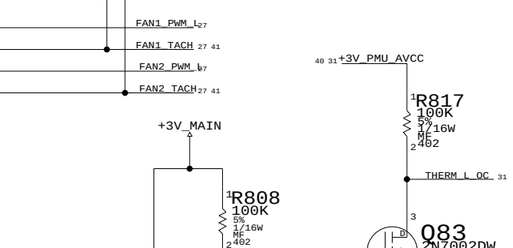


CPU FAN



GPU FAN





FAN/MODEM/SOUND/BACKUP BATT.

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SCALE NONE	SHT 27 OF 46	

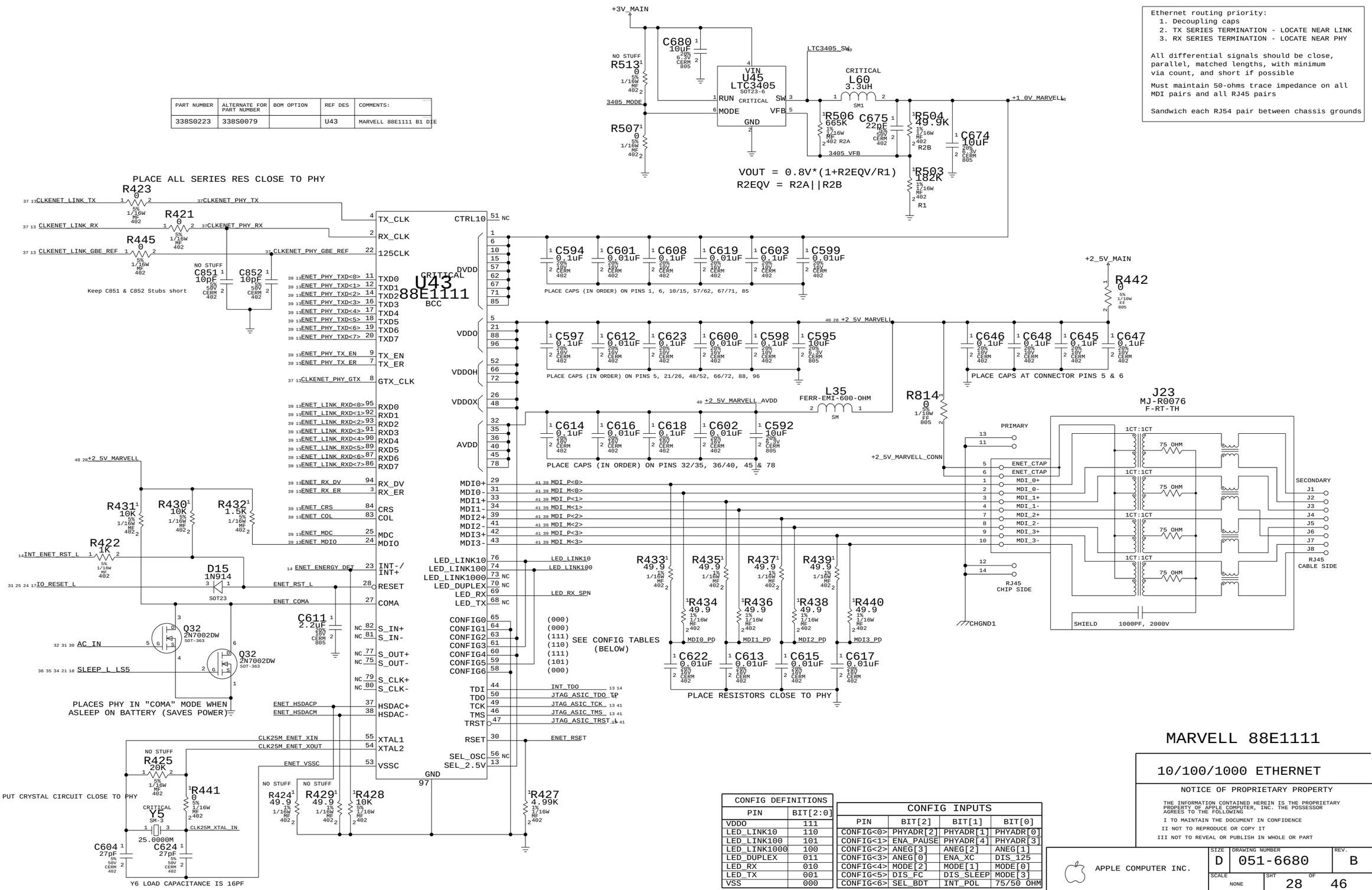
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S0223	338S0079		U43	MARVELL 88E1111 B1 DIE

Ethernet routing priority:
1. Decoupling caps
2. TX SERIES TERMINATION - LOCATE NEAR LINK
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds



CONFIG DEFINITIONS	
PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG INPUTS			
PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM

MARVELL 88E1111

10/100/1000 ETHERNET

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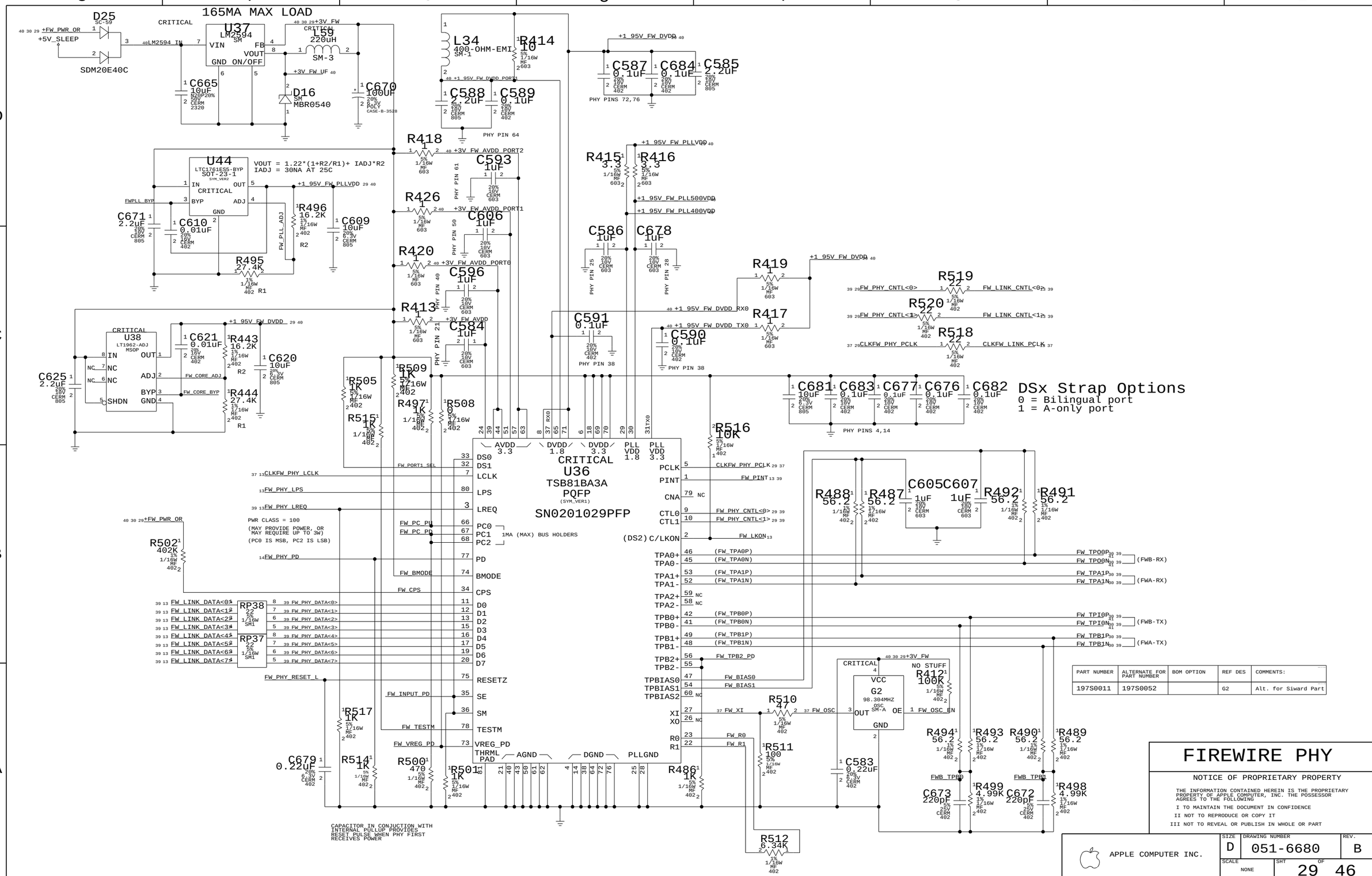
SIZE	DRAWING NUMBER	REV.
D	051-6680	B
SCALE NONE	SHT 28 OF 46	



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0011	197S0052		G2	Alt. for Siward Part

FIREWIRE PHY

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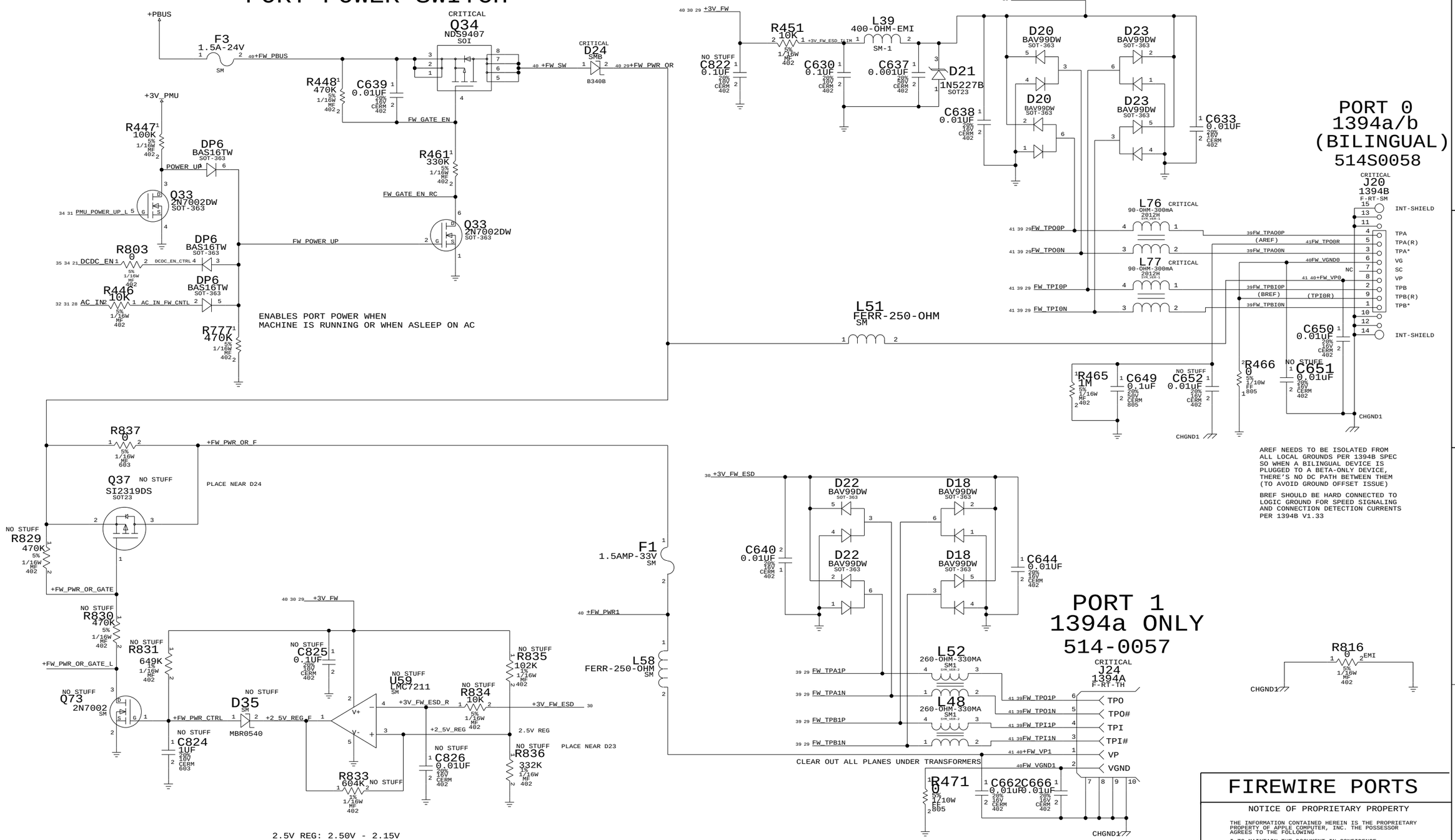
PORT POWER SWITCH



FIREWIRE PORTS

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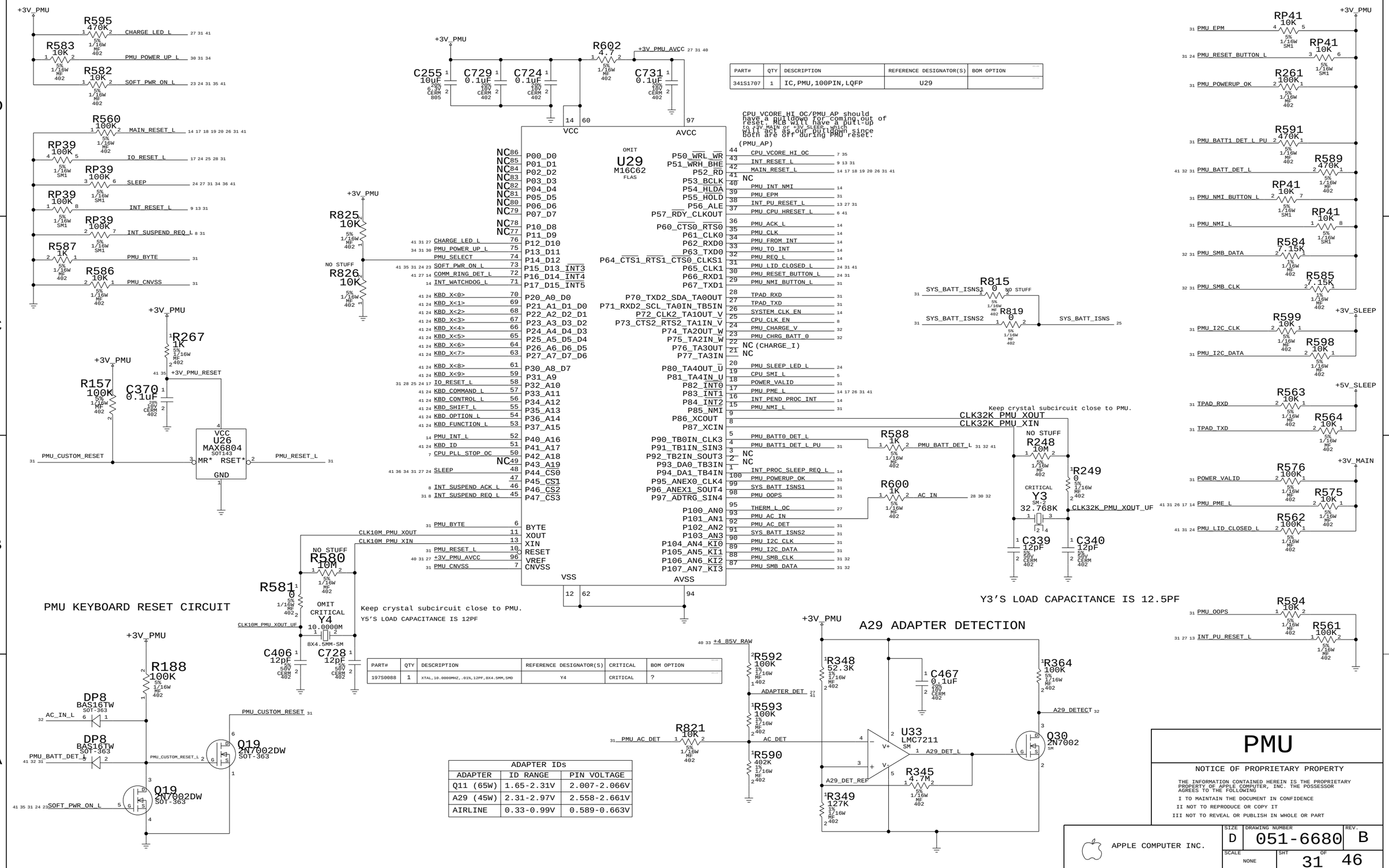
SCALE NONE	SHT 30 OF 46	

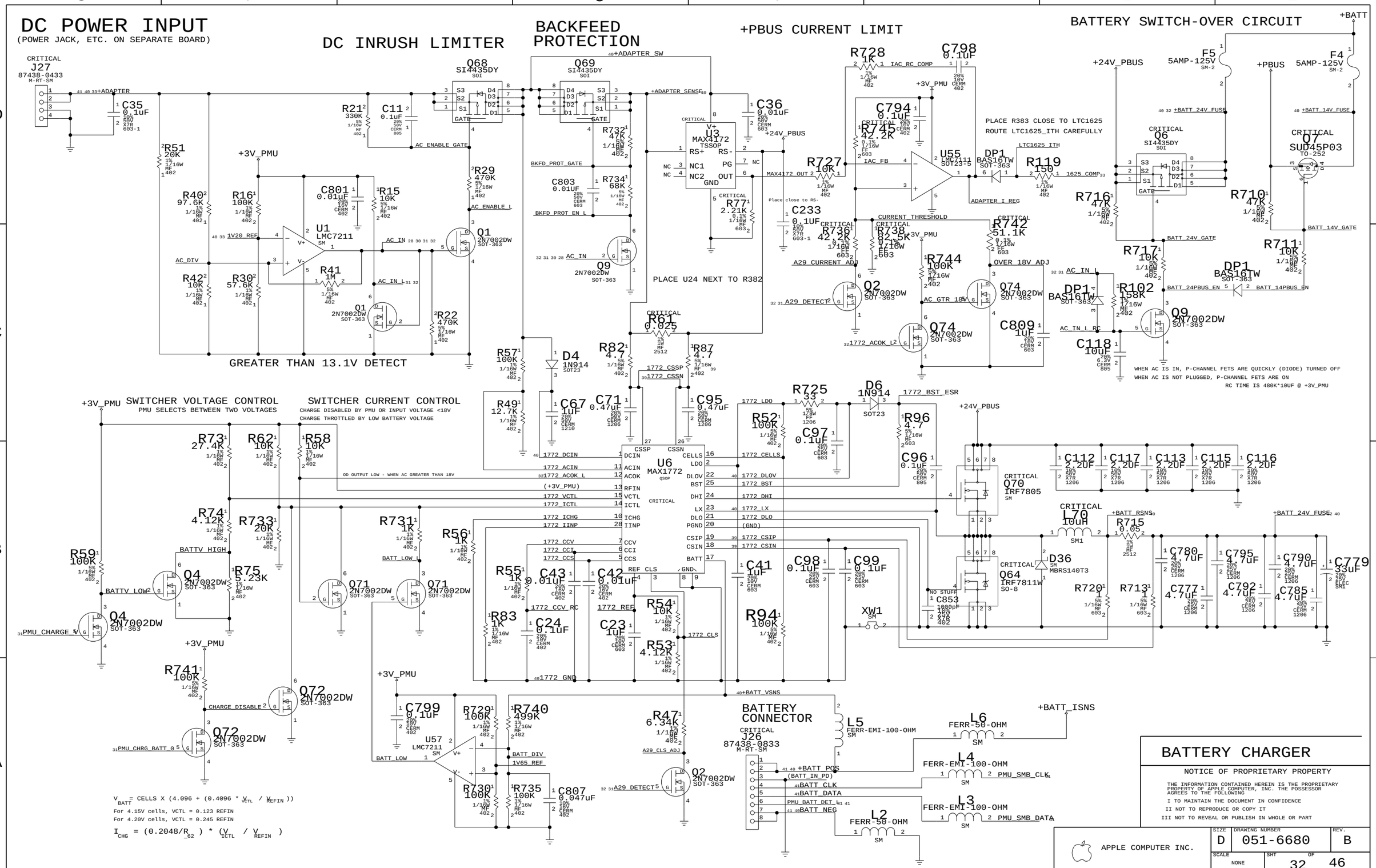


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1707	1	IC,PMU,100PIN,LQFP	U29	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0088	1	XTAL,10.0000MHZ,.01%,12PF,8X4.5MM,SMD	Y4	CRITICAL	?

ADAPTER IDs

ADAPTER	ID RANGE	PIN VOLTAGE
Q11 (65W)	1.65-2.31V	2.007-2.066V
A29 (45W)	2.31-2.97V	2.558-2.661V
AIRLINE	0.33-0.99V	0.589-0.663V


DC POWER INPUT
(POWER JACK, ETC. ON SEPARATE BOARD)
DC INRUSH LIMITER
BACKFEED PROTECTION
+PBUS CURRENT LIMIT
BATTERY SWITCH-OVER CIRCUIT
GREATER THAN 13.1V DETECT
SWITCHER VOLTAGE CONTROL
PMU SELECTS BETWEEN TWO VOLTAGES
SWITCHER CURRENT CONTROL
CHARGE DISABLED BY PMU OR INPUT VOLTAGE <18V
CHARGE THROTTLED BY LOW BATTERY VOLTAGE
OD OUTPUT LOW - WHEN AC GREATER THAN 18V
PLACE U24 NEXT TO R382
PLACE R383 CLOSE TO LTC1625
ROUTE LTC1625_ITH CAREFULLY
WHEN AC IS IN, P-CHANNEL FETS ARE QUICKLY (DIODE) TURNED OFF
WHEN AC IS NOT PLUGGED, P-CHANNEL FETS ARE ON
RC TIME IS 480K*10UF @ +3V_PMU
BATTERY CONNECTOR
BATTERY CHARGER
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SIZE D
DRAWING NUMBER 051-6680
REV. B
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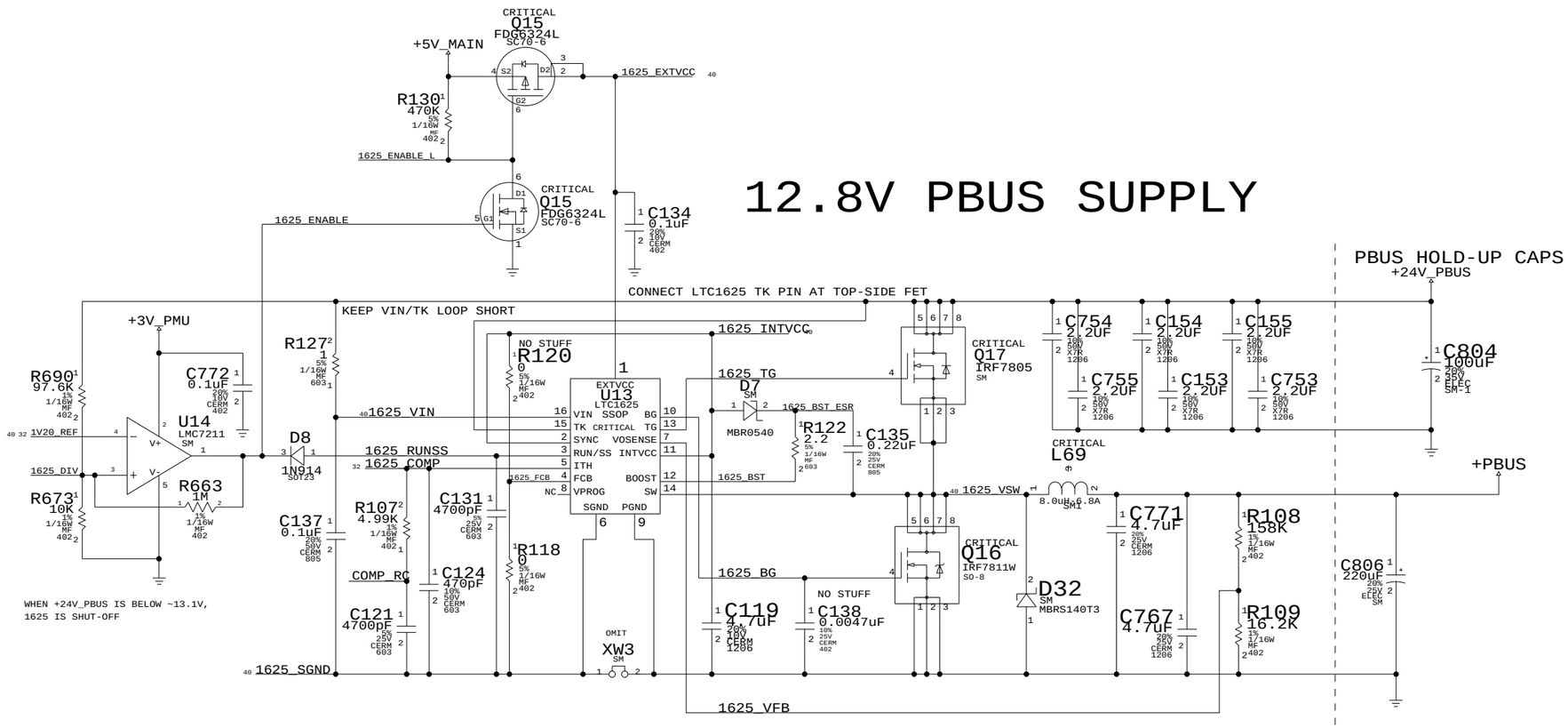
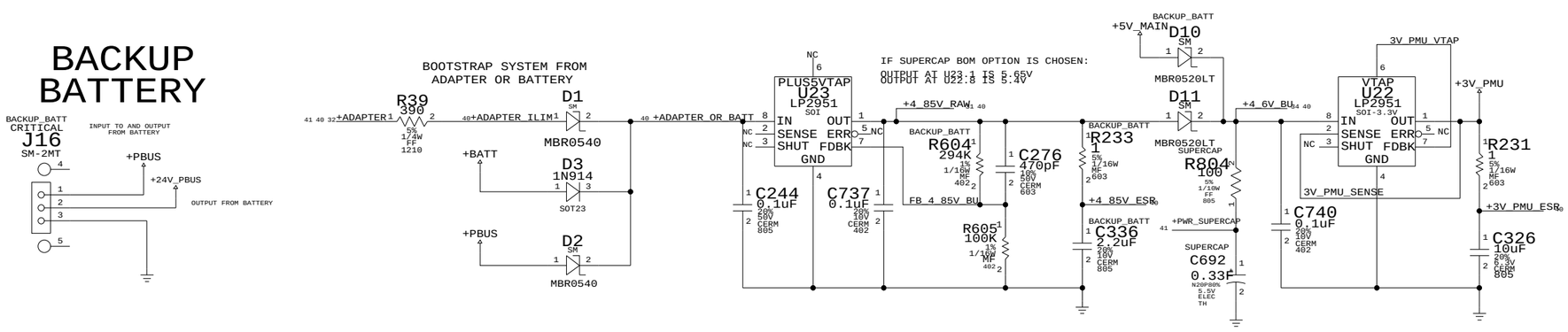
12.8V PBUS SUPPLY



PMU SUPPLY



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S3575	1	RES,MF,1/16W,357K OHM,1%,0402,SMD	R604	?	SUPERCAP

12.8V REGULATOR

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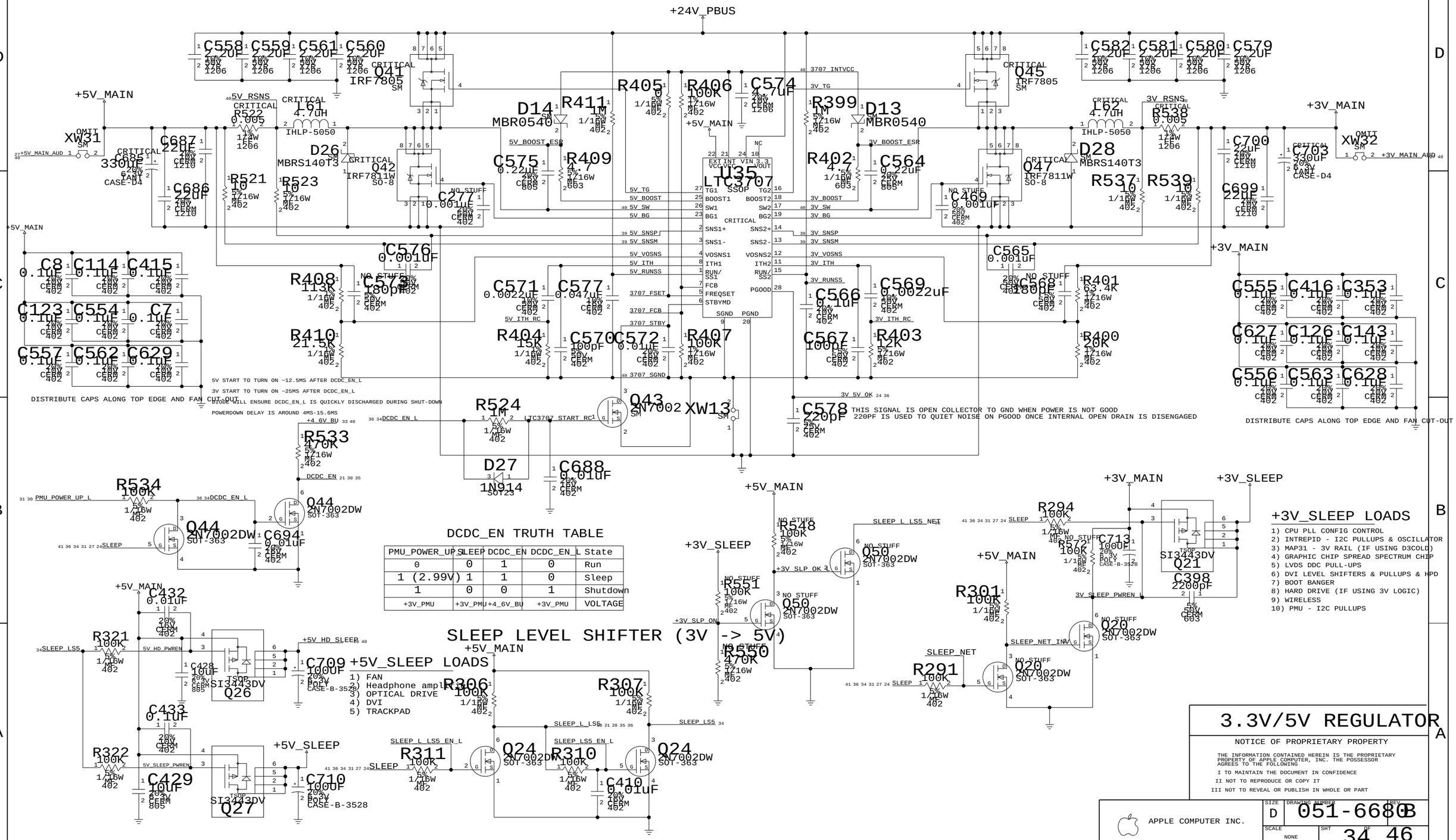
3.3V/5V MAIN SUPPLY



PMU_POWER_UP_L	SLEEP	DCDC_EN	DCDC_EN_L	State
0	0	1	0	Run
1 (2.99V)	1	1	0	Sleep
1	0	0	1	Shutdown
+3V_PMU	+3V_PMU	+4_6V_BU	+3V_PMU	VOLTAGE

3.3V/5V REGULATOR

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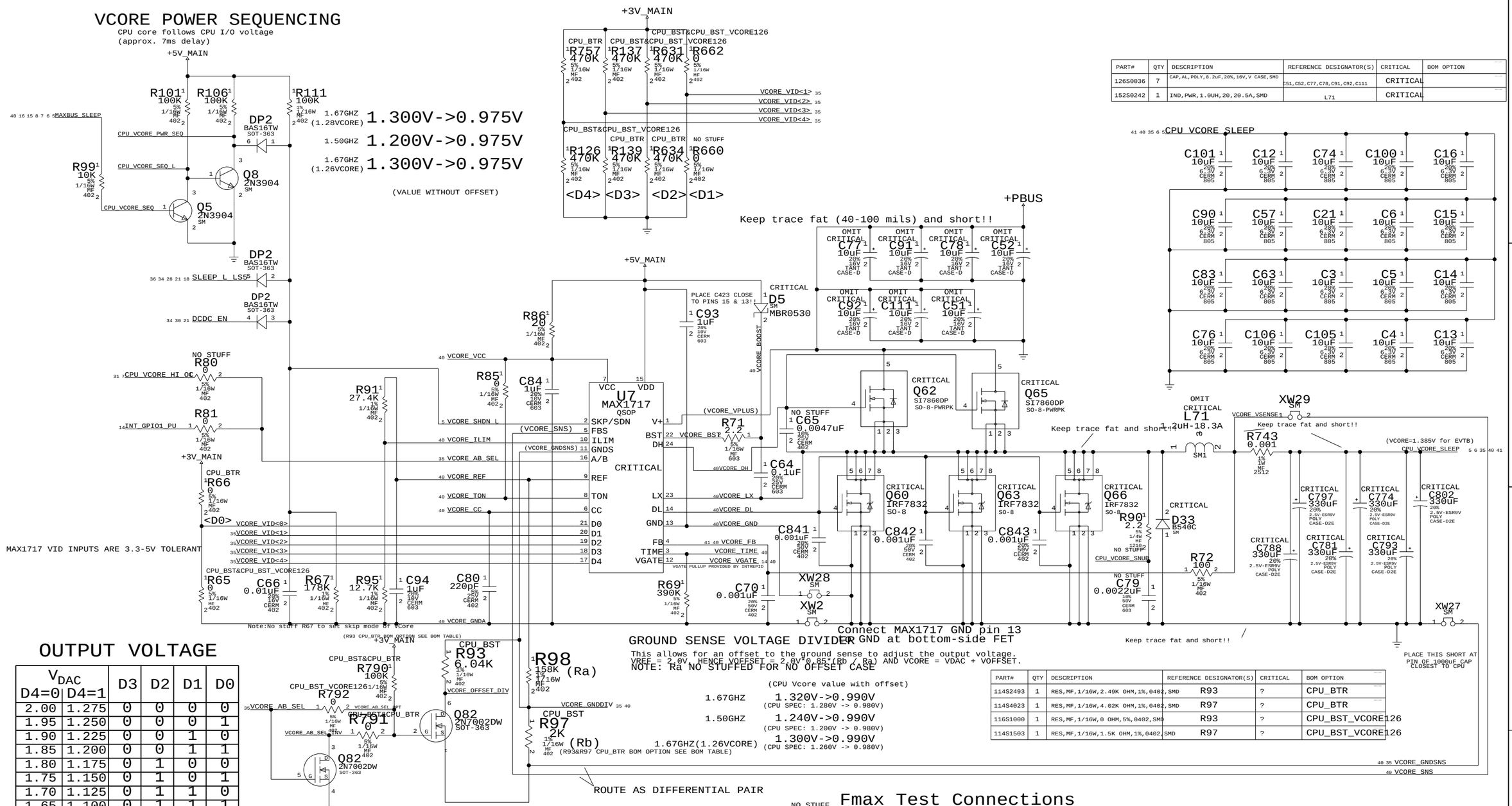
VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage
(approx. 7ms delay)

1.67GHZ (1.28VCORE) 1.300V->0.975V
1.50GHZ 1.200V->0.975V
1.67GHZ (1.26VCORE) 1.300V->0.975V

(VALUE WITHOUT OFFSET)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
126S0036	7	CAP,AL,POLY,8.2uF,20%,16V,V CASE,SMD	C51,C52,C77,C78,C91,C92,C111	CRITICAL	
152S0242	1	IND,PWR,1.0UH,20,20.5A,SMD	L71	CRITICAL	

OUTPUT VOLTAGE

V_{DAC} D4=0	V_{DAC} D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

FOR V-STEP:

D<4..0>	A/B_ = Hi/Fast	A/B_ = Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1

If all pull-ups are >=100K and all
pull-downs are <=1K, V = VA. B

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
VREF = 2.0V, HENCE VOFFSET = 2.0V*0.85*(Rb / Ra) AND VCORE = VDAC + VOFFSET.
NOTE: Ra NOT STUFFED FOR NO OFFSET CASE

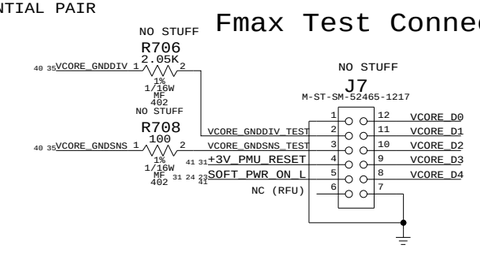
(CPU Vcore value with offset)

1.67GHZ 1.320V->0.990V (CPU SPEC: 1.280V -> 0.980V)
1.50GHZ 1.240V->0.990V (CPU SPEC: 1.200V -> 0.980V)
1.67GHZ(1.26VCORE) 1.300V->0.990V (CPU SPEC: 1.260V -> 0.980V)

(R93&R97 CPU_BTR BOM OPTION SEE BOM TABLE)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S2493	1	RES,MF,1/16W,2.49K OHM,1%,0402,SMD	R93	?	CPU_BTR
114S4023	1	RES,MF,1/16W,4.02K OHM,1%,0402,SMD	R97	?	CPU_BTR
116S1000	1	RES,MF,1/16W,0 OHM,5%,0402,SMD	R93	?	CPU_BST_VCORE126
114S1503	1	RES,MF,1/16W,1.5K OHM,1%,0402,SMD	R97	?	CPU_BST_VCORE126

Fmax Test Connections



VCORE SUPPLY

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1.5V/2.5V SWITCHER

+1_5V_SLEEP LOADS
1) AGP I/O - IF USING D3COLD
2) MAXBUS I/O - IF 1.5V INTERFACE

+1_5V_MAIN LOADS
1) INTREPID CORE

+2_5V_MAIN LOADS
1) MAP31 - FBCORE/FBIO IF USING D3HOT
2) GIGABIT ETHERNET - AVDDL
3) DDR SODIMMS - CORE/IO
4) DDR MUXES

M11 Power Shut down Sequencing

+2_5V_SLEEP LOADS
1) FBCORE/FBIO IF USING D3COLD

1.8V SWITCHER

+1_8V_MAIN LOADS
1) INTREPID PLLS

+1_8V_SLEEP LOADS
1) MPC7447 - MAXBUS I/O - IF 1.8V INTERFACE
2) CPU JTAG & MaxBus Pull-ups
3) CPU PLL Config Straps

1.5V/1.8V/2.5V SUPPLIES

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DIGITAL SIGNALS

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM
				STUB_LENGTH OF 200 MILS NEEDED WHEN WE CONVERT TO 14.2				
GROUP 0	MEM_DATA<7..0>	L:S:1602:1700	7	500	(200)			167 MHZ
	MEM_DQM<0>	L:S:1602 MIL:1700 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<0>	L:S:1602 MIL:1700 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<7..0>	L:S:1903:2000	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<0>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<0>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<7..0>	L:S:2000:2100	7	500	(200)			167 MHZ
	RAM_DQM_B<0>	L:S:2000 MIL:2100 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<0>	L:S:2000 MIL:2100 MIL	7	500.0000	(200)			167.0 MHz
GROUP 1	MEM_DATA<15..8>	L:S:1344:1660	7	500	(200)			167 MHZ
	MEM_DQM<1>	L:S:1344 MIL:1660 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<1>	L:S:1344 MIL:1660 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<15..8>	L:S:1905:2000	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<1>	L:S:1905 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<1>	L:S:1905 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<15..8>	L:S:2004:2412	7	500	(200)			167 MHZ
	RAM_DQM_B<1>	L:S:2004 MIL:2412 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<1>	L:S:2004 MIL:2412 MIL	7	500.0000	(200)			167.0 MHz
GROUP 2	MEM_DATA<23..16>	L:S:1435:1500	7	500	(200)			167 MHZ
	MEM_DQM<2>	L:S:1435 MIL:1500 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<2>	L:S:1435 MIL:1500 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<23..16>	L:S:1707:1800	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<2>	L:S:1707 MIL:1800 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<2>	L:S:1707 MIL:1800 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<23..16>	L:S:1900:2000	7	500	(200)			167 MHZ
	RAM_DQM_B<2>	L:S:1900 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<2>	L:S:1900 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
GROUP 3	MEM_DATA<31..24>	L:S:1233:1485	7	500	(200)			167 MHZ
	MEM_DQM<3>	L:S:1233 MIL:1485 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<3>	L:S:1233 MIL:1485 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<31..24>	L:S:1700:2165	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<3>	L:S:1700 MIL:2165 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<3>	L:S:1700 MIL:2165 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<25..24>	L:S:1907:2356	7	500	(200)			167 MHZ
	RAM_DATA_B<26>	L:S:1907 MIL:2356 MIL	7		(200)			167.0 MHz
	RAM_DATA_B<31..27>	L:S:1907:2356	7	500	(200)			167 MHZ
	RAM_DQM_B<3>	L:S:1907 MIL:2356 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<3>	L:S:1907 MIL:2356 MIL	7	500.0000	(200)			167.0 MHz
GROUP 4	MEM_DATA<39..32>	L:S:1915:2000	7	500	(200)			167 MHZ
	MEM_DQM<4>	L:S:1915 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<4>	L:S:1915 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<39..32>	L:S:1205:1387	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
DDR RAM	RAM_DQM_A<4>	L:S:1205 MIL:1387 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<4>	L:S:1205 MIL:1387 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<39..32>	L:S:1404:1686	7	500	(200)			167 MHZ
	RAM_DQM_B<4>	L:S:1404 MIL:1686 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<4>	L:S:1404 MIL:1686 MIL	7	500.0000	(200)			167.0 MHz
GROUP 5	MEM_DATA<47..40>	L:S:1719:1893	7	500	(200)			167 MHZ
	MEM_DQM<5>	L:S:1719 MIL:1893 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<5>	L:S:1719 MIL:1893 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<47..40>	L:S:1607:1898	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<5>	L:S:1607 MIL:1898 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<5>	L:S:1607 MIL:1898 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<47..40>	L:S:1716:2102	7	500	(200)			167 MHZ
	RAM_DQM_B<5>	L:S:1716 MIL:2102 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<5>	L:S:1716 MIL:2102 MIL	7	500.0000	(200)			167.0 MHz
GROUP 6	MEM_DATA<55..48>	L:S:2101:2170	7	500	(200)			167 MHZ
	MEM_DQM<6>	L:S:2101 MIL:2170 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<6>	L:S:2101 MIL:2170 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<55..48>	L:S:1204:1357	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<6>	L:S:1204 MIL:1357 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<6>	L:S:1204 MIL:1357 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<55..48>	L:S:1400:1546	7	500	(200)			167 MHZ
	RAM_DQM_B<6>	L:S:1400 MIL:1546 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<6>	L:S:1400 MIL:1546 MIL	7	500.0000	(200)			167.0 MHz
GROUP 7	MEM_DATA<63..56>	L:S:1903:2000	7	500	(200)			167 MHZ
	MEM_DQM<7>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<7>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<63..56>	L:S:1611:1696	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<7>	L:S:1611 MIL:1696 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<7>	L:S:1611 MIL:1696 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<63..56>	L:S:1809:1887	7	500	(200)			167 MHZ
	RAM_DQM_B<7>	L:S:1809 MIL:1887 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<7>	L:S:1809 MIL:1887 MIL	7	500.0000	(200)			167.0 MHz
ADDR	MEM_ADDR<12..0>	L:S::500	4					83 MHZ
	RAM_ADDR<12..0>	L:S:2000:3000	10		(200)			
	MEM_BA<1..0>	L:S::500	4					
	RAM_BA<1..0>	L:S:2000:3300	8		(200)			
CONTROL	MEM_CS_L<3..0>	L:S::500	4					
	RAM_CS_L<3..0>	L:S:2500:3200	7		(200)			
	MEM_CKE<3..0>	L:S::500	4					
	RAM_CKE<3..0>	L:S:2500:3200	7		(200)			
	MEM_RAS_L	L:S::500 MIL	4					
	RAM_RAS_L	L:S:2000 MIL:4100 MIL	7		(200)			
	MEM_CAS_L	L:S::500 MIL	4					
	RAM_CAS_L	L:S:2000 MIL:4100 MIL	7		(200)			
	MEM_WE_L	L:S::500 MIL	4					
	RAM_WE_L	L:S:2000 MIL:3100 MIL	8		(200)			
	MEM_MUXSEL_MSB	L:S:1700 MIL:3000 MIL	8					
	MEM_MUXSEL_LSB	L:S:1700 MIL:3000 MIL	7					

PRIORITY: 2
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9
GOAL: MINIMIZE
EXPOSED ROUTES
MINIMIZE VIAS

CLOCK LINE CONSTRAINTS

GROUP	SIG_NAME	PROPAGATION_DELAY	MATCHED_DELAY	MAX VIAS	MAX EXPOSED LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE PARAM
INTREPID CLOCKS	SYSCLK_CPU_UF	L:S::150 MIL					10 MIL SPACING	167.0 MHz
	SYSCLK_CPU	L:S:2650 MIL:2750 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz
	INT_CPUFB_OUT	L:S::150 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_OUT_SHORT	L:S:700 MIL:850 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_OUT_NORM	L:S:500 MIL:600 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_IN_NORM	L:S:500 MIL:600 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_LONG	L:S:1050 MIL:1150 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_IN	L:S:700 MIL:800 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0_UF	L:S:300 MIL:350 MIL	SYSCLK_DDRCLK_A0_UF:G:L:S:0 MIL:25 MIL	4		(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0	L:S:300 MIL:350 MIL	SYSCLK_DDRCLK_A0_UF:G:L:S:0 MIL:25 MIL	4		(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1_UF	L:S:300 MIL:350 MIL	SYSCLK_DDRCLK_A1_UF:G:L:S:0 MIL:25 MIL	4		(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1	L:S:300 MIL:350 MIL	SYSCLK_DDRCLK_A1_UF:G:L:S:0 MIL:25 MIL	4		(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0_UF	L:S:300 MIL:350 MIL	SYSCLK_DDRCLK_B0_UF:G:L:S:0 MIL:25 MIL	4		(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0	L:S:300 MIL:350 MIL	SYSCLK_DDRCLK_B0_UF:G:L:S:0 MIL:25 MIL	4		(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1_UF	L:S:300 MIL:350 MIL	SYSCLK_DDRCLK_B1_UF:G:L:S:0 MIL:25 MIL	4		(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1	L:S:300 MIL:350 MIL	SYSCLK_DDRCLK_B1_UF:G:L:S:0 MIL:25 MIL	4		(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A0:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A0:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A1:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A1:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B0:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B0:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B1:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B1:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	INT_REF_CLK_OUT_UF	L:S::400 MIL				(200)	10 MIL SPACING	49.92 MHz
	INT_REF_CLK_OUT	L:S:1000 MIL:1150 MIL		5	250.0000	(200)	10 MIL SPACING	49.92 MHz
	INT_REF_CLK_IN	L:S:1900 MIL:2000 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz
	CLK66M_GPU_AGP_UF	L:S::150 MIL				(200)	10 MIL SPACING	66.00 MHz
	CLK66M_GPU_AGP	L:S:1800 MIL:1900 MIL		6	400.0000	(200)	10 MIL SPACING	66.00 MHz
	INT_AGP_FB_OUT	L:S::150 MIL				(200)	10 MIL SPACING	66.00 MHz
	INT_AGP_FB_IN	L:S:1450 MIL:1550 MIL		6	500.0000	(200)	10 MIL SPACING	66.00 MHz
	CLK33M_CBUS_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz
	CLK33M_CBUS	L:S:5000 MIL:6000 MIL		9	500.0000	(200)	10 MIL SPACING	33.00 MHz
	CLK33M_AIRPORT_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz
	CLK33M_AIRPORT	L:S:9500 MIL:10500 MIL		6	500.0000	(200)	10 MIL SPACING	33.00 MHz
	CLK33M_NEC_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz
	CLK33M_NEC	L:S:4000 MIL:6000 MIL		7	500.0000	(200)	10 MIL SPACING	33.00 MHz
	INT_PCI_FB_OUT	L:S::300 MIL				(200)	10 MIL SPACING	33.00 MHz
	INT_PCI_FB_IN	L:S:6500 MIL:7500 MIL		7	500.0000	(200)	10 MIL SPACING	33.00 MHz
M11 & OSC	ATI_CLK27M_OSC	L:S::400 MIL		5		(200)	10 MIL SPACING	
	ATI_CLK27M_OSC_SS	L:S::400 MIL		5		(200)	10 MIL SPACING	
	ATI_CLK27M_IN	L:S::200 MIL		5		(200)	10 MIL SPACING	
	ATI_SSCLK_UF	L:S::200 MIL		5		(200)	10 MIL SPACING	
	ATI_SSCLK_IN	L:S::1800 MIL		5	500.0000	(200)	10 MIL SPACING	
CRYSTALS	CLK18M_INT_XIN	L:S:1400 MIL:1500 MIL					10 MIL SPACING	
	CLK18M_INT_XOUT	L:S:1250 MIL:1350 MIL					10 MIL SPACING	
	CLK18M_XTAL_IN	L:S::300 MIL					10 MIL SPACING	
	CLK18M_INT_EXT	L:S::400 MIL					10 MIL SPACING	
SOUND	INT_I2S0_SND_MCLK			6	500.0000	(200)	10 MIL SPACING	
ETHERNET	CLKENET_PHY_RX	L:S::300 MIL				(200)		125.0 MHz
	CLKENET_LINK_RX	L:S:8000 MIL:9000 MIL		6	800.0000	(200)	10 MIL SPACING	125.0 MHz
	CLKENET_PHY_GBE_REF	L:S::300 MIL				(200)		125.0 MHz
	CLKENET_LINK_GBE_REF	L:S:8000 MIL:9000 MIL		6	500.0000	(200)	10 MIL SPACING	125.0 MHz
	CLKENET_PHY_TX	L:S::300 MIL				(200)		25.00 MHz
	CLKENET_LINK_TX	L:S:8000 MIL:9000 MIL		6	500.0000	(200)	10 MIL SPACING	25.00 MHz
	CLKENET_LINK_GTX	L:S::300 MIL				(200)		125.0 MHz
	CLKENET_PHY_GTX	L:S:8000 MIL:9000 MIL		6	600.0000	(200)	10 MIL SPACING	125.0 MHz
FIREWIRE	CLKFW_PHY_PCLK	L:S::300 MIL				(200)		49.15 MHz
	CLKFW_LINK_PCLK	L:S:7500 MIL:8000 MIL		5	500.0000	(200)	10 MIL SPACING	49.15 MHz
	CLKFW_PHY_LCLK	L:S:7500 MIL:8000 MIL		5	500.0000	(200)	10 MIL SPACING	49.15 MHz
	CLKFW_LINK_LCLK	L:S::300 MIL				(200)		49.15 MHz
	FW_XI	L:S::500 MIL				(200)	10 MIL SPACING	98.03 MHz
	FW_OSC	L:S::300 MIL				(200)	10 MIL SPACING	98.03 MHz

PRIORITY: 1
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9
GOAL: MINIMIZE EXPOSURE ON LONG NETS

SIGNAL CONSTRAINTS - PAGE 1

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	B
SCALE NONE	SHT 37 OF 46	

DIGITAL SIGNALS

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
MAXBUS	CPU_AACK_L	L:S:1500 MIL:2700	MIL7		(250)				5 8
	CPU_ADDR<0..31>	L:S:1500:3100	7		(250)		TRUE	83 MHZ	5 8
	CPU_ARTRY_L	L:S:1500 MIL:2700	MIL7		(250)				5 8
	CPU_BG_L	L:S:1500 MIL:2700	MIL7		(250)				5 8
	CPU_BR_L	L:S:1500 MIL:2700	MIL7		(250)				5 8
	CPU_CI_L	L:S:1500 MIL:2700	MIL7		(250)				5 8
	CPU_DATA<0..31>	L:S:1100:2700	7		(250)		TRUE	83 MHZ	6 8
	CPU_DATA<32..63>	L:S:1100:2700	8		(250)			83 MHZ	6 8
	CPU_DBG_L	L:S:1500 MIL:2700	MIL7		(250)				5 8
	CPU_DTI<0..2>	L:S:1500:2950	7		(250)				5 8
	CPU_DRDY_L	L:S:1500 MIL:3200	MIL7		(250)				5 8
	CPU_GBL_L	L:S:1500 MIL:2700	MIL7		(250)				5 8
	CPU_HIT_L	L:S:1500 MIL:2800	MIL7		(250)				5 8
	CPU_QACK_L	L:S:1500 MIL:2700	MIL7		(250)				5 8
	CPU_QREQ_L	L:S:1500 MIL:2700	MIL7		(250)				5 8
	CPU_TA_L	L:S:1500 MIL:2700	MIL7		(250)				5 8
	CPU_TBST_L	L:S:1500 MIL:2700	MIL7		(250)				5 8
	CPU_TEA_L	L:S:1500 MIL:3000	MIL7		(250)				5 8
	CPU_TS_L	L:S:1500 MIL:2700	MIL7		(250)				5 8
	CPU_TSIZ<0..2>	L:S:1500:3500	7		(250)				5 8
	CPU_TT<0..4>	L:S:1500:3400	7		(250)				5 8
	CPU_WT_L	L:S:1500 MIL:3100	MIL7		(250)				5 8

PRIORITY: 4
PRIMARY LAYERS: 9
SECONDARY LAYERS: 4,7
GOAL: MINIMIZE TH VIAS

STUB_LENGTH OF 250 MILS NEEDED WHEN DESIGN SWITCHED TO 14.2

TMDS/DVO SIGNAL CONSTRAINTS

ALL TMDS GROUP SIGNALS ROUTE AT LAYER 4 OR 7 AND HAVE SAME WIDTH SPACING RULE AS OTHER TMDS SIGNALES

SI_TMDS_CLKN	SI_CLKTMDS	SITMDS:G:L:S:0 MIL:300 MIL		100 OHM SPACING FOR TMDS	20
SI_TMDS_CLKP	SI_CLKTMDS	SITMDS:G:L:S:0 MIL:300 MIL		100 OHM SPACING FOR TMDS	20
SI_TMDS_DN<0>	SI_TMDS_D0			100 OHM SPACING FOR TMDS	20
SI_TMDS_DP<0>	SI_TMDS_D0			100 OHM SPACING FOR TMDS	20
SI_TMDS_DN<1>	SI_TMDS_D1			100 OHM SPACING FOR TMDS	20
SI_TMDS_DP<1>	SI_TMDS_D1			100 OHM SPACING FOR TMDS	20
SI_TMDS_DN<2>	SI_TMDS_D2			100 OHM SPACING FOR TMDS	20
SI_TMDS_DP<2>	SI_TMDS_D2			100 OHM SPACING FOR TMDS	20
SI_TMDS_DN<3>	SI_TMDS_D3			100 OHM SPACING FOR TMDS	20
SI_TMDS_DP<3>	SI_TMDS_D3			100 OHM SPACING FOR TMDS	20
SI_TMDS_DN<4>	SI_TMDS_D4			100 OHM SPACING FOR TMDS	20
SI_TMDS_DP<4>	SI_TMDS_D4			100 OHM SPACING FOR TMDS	20
SI_TMDS_DN<5>	SI_TMDS_D5			100 OHM SPACING FOR TMDS	20
SI_TMDS_DP<5>	SI_TMDS_D5			100 OHM SPACING FOR TMDS	20

ALL THE DVOD GROUP SIGNALS ROUTE AT LAYER 4 OR 7 AND ROUTE AS STANDARD 50OHM SIGNALS AT 4 MILS

ATI_DVOD<23..0>	ATIDVOD:G:L:S:1600 MIL:1700 MIL	6	610		20	21
ATI_DVOD_DE	ATIDVOD:G:L:S:1600 MIL:1700 MIL	6	610.0000		20	21
ATI_DVO_HSYNC	ATIDVOD:G:L:S:1600 MIL:1700 MIL	6	610.0000		20	21
ATI_DVO_VSYNC	ATIDVOD:G:L:S:1600 MIL:1700 MIL	6	610.0000		20	21
ATI_DVO_CLKP	ATIDVOD:G:L:S:0 MIL:500 MIL	6	610.0000	165.0 MHz:::	19	21
GPU_DVO_CLKP_R1	ATIDVOD:G:L:S:0 MIL:1100 MIL	6	610.0000	165.0 MHz:::	19	20
GPU_DVO_CLKP_R2	ATIDVOD:G:L:S:0 MIL:1100 MIL	6	610.0000	165.0 MHz:::	19	20

TMDS_CONN_CLKN	CLKCONN_TMDS	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING FOR TMDS		
TMDS_CONN_CLKP	CLKCONN_TMDS	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING FOR TMDS	23	41
TMDS_CONN_DN<0>	CONN_TMDS_D0		500.0000	100 OHM SPACING FOR TMDS		
TMDS_CONN_DP<0>	CONN_TMDS_D0		500.0000	100 OHM SPACING FOR TMDS		
TMDS_CONN_DN<1>	CONN_TMDS_D1		500.0000	100 OHM SPACING FOR TMDS		
TMDS_CONN_DP<1>	CONN_TMDS_D1		500.0000	100 OHM SPACING FOR TMDS		
TMDS_CONN_DN<2>	CONN_TMDS_D2		500.0000	100 OHM SPACING FOR TMDS		
TMDS_CONN_DP<2>	CONN_TMDS_D2		500.0000	100 OHM SPACING FOR TMDS	23	

TMDS_DN<3>	TMDS_D3		500.0000	100 OHM SPACING FOR TMDS		
TMDS_DP<3>	TMDS_D3		500.0000	100 OHM SPACING FOR TMDS		
TMDS_DN<4>	TMDS_D4		500.0000	100 OHM SPACING FOR TMDS		
TMDS_DP<4>	TMDS_D4		500.0000	100 OHM SPACING FOR TMDS		
TMDS_DN<5>	TMDS_D5		500.0000	100 OHM SPACING FOR TMDS		
TMDS_DP<5>	TMDS_D5		500.0000	100 OHM SPACING FOR TMDS	20	23
TMDS_CONN_DN<3>	CONN_TMDS_D3		500.0000	100 OHM SPACING FOR TMDS		
TMDS_CONN_DP<3>	CONN_TMDS_D3		500.0000	100 OHM SPACING FOR TMDS		
TMDS_CONN_DN<4>	CONN_TMDS_D4		500.0000	100 OHM SPACING FOR TMDS		
TMDS_CONN_DP<4>	CONN_TMDS_D4		500.0000	100 OHM SPACING FOR TMDS		
TMDS_CONN_DN<5>	CONN_TMDS_D5		500.0000	100 OHM SPACING FOR TMDS		
TMDS_CONN_DP<5>	CONN_TMDS_D5		500.0000	100 OHM SPACING FOR TMDS	23	

GPU_R	GPU_R	500.0000	100 OHM SPACING	21	23
GPU_G	GPU_G	500.0000	100 OHM SPACING	21	23
GPU_B	GPU_B	500.0000	100 OHM SPACING	21	23

SIGNAL CONSTRAINTS - PAGE 1

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SIZE	DRAWING NUMBER	REV.
D	051-6680	B
SCALE NONE	SHT 38 OF 46	

Digital Signals (cont'd)

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
AGP	AGP_AD<15..0>	L:S:1050:1450	7					66 MHZ	12 19
AGP BYTES 0-1	AGP_CBE<1..0>	L:S:1050:1450	7					66 MHZ	12 19
	AGP_AD_STB<0>	L:S:1050 MIL:1450 MIL	4		(250)	8 MIL SPACING		133.0 MHZ	12 19
	AGP_AD_STB_L<0>	L:S:1050 MIL:1450 MIL	4		(250)	8 MIL SPACING		133.0 MHZ	12 19
AGP BYTES 2-3	AGP_AD<31..16>	L:S:1050:1450	7					66 MHZ	12 19
	AGP_CBE<3..2>	L:S:1050:1450	7					66 MHZ	12 19
	AGP_AD_STB<1>	L:S:1050 MIL:1450 MIL	4		(250)	8 MIL SPACING		133.0 MHZ	12 19
	AGP_AD_STB_L<1>	L:S:1050 MIL:1450 MIL	4		(250)	8 MIL SPACING		133.0 MHZ	12 19
AGP SIDEBAND	AGP_SBA<7..0>	L:S:1050:1450	7					66 MHZ	12 19
	AGP_SB_STB	L:S:1050 MIL:1450 MIL	4		(350)	8 MIL SPACING		66.00 MHZ	12 19
	AGP_SB_STB_L	L:S:1050 MIL:1450 MIL	4		(350)	8 MIL SPACING		66.00 MHZ	12 19
AGP CONTROL	AGP_FRAME_L	L:S:1250 MIL:1950 MIL	4					66.00 MHZ	12 19
	AGP_IRDY_L	L:S:1250 MIL:1950 MIL	4					66.00 MHZ	12 19
	AGP_TRDY_L	L:S:1250 MIL:1950 MIL	4					66.00 MHZ	12 19
	AGP_DEVSEL_L	L:S:1250 MIL:1950 MIL	4					66.00 MHZ	12 19
	AGP_STOP_L	L:S:1250 MIL:1950 MIL	4					66.00 MHZ	12 19
	AGP_PAR	L:S:1250 MIL:1950 MIL	4					66.00 MHZ	12 19
	AGP_REQ_L	L:S:1250 MIL:1950 MIL	4					66.00 MHZ	12 19
	AGP_GNT_L	L:S:1250 MIL:1950 MIL	4					66.00 MHZ	12 19
	AGP_RBF_L	L:S:1250 MIL:1950 MIL	4					66.00 MHZ	12 19
PCI	PCI_AD<31..0>	L:S:6000:12500				MIN_DAISY_CHAIN		33 MHZ	9,12 17 18 26 41
	PCI_CBE<3..0>	L:S:6000:12500				MIN_DAISY_CHAIN		33 MHZ	12 17 18 26
	PCI_FRAME_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ	12 17 18 26 41
	PCI_IRDY_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ	12 17 18 26 41
	PCI_TRDY_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ	12 17 18 26 41
	PCI_DEVSEL_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ	12 17 18 26 41
	PCI_STOP_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ	12 17 18 26 41
	PCI_PAR	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ	12 17 18 26 41
ULTRA ATA-100	UIDE_DATA<15..8>	L:S::710			(200)			100 MHZ	13 26
	UIDE_DATA<7>	U51.V1:RP19.3::600 MIL			(200)			100.0 MHZ	13 26
	UIDE_DATA<6..0>	L:S::600			(200)			100 MHZ	13 26
	UIDE_ADDR<2..0>	L:S::650			(200)	NEED TO MATCH DELAY TO 250		100 MHZ	13 26
	UIDE_RST_L	L:S::400 MIL			(200)			100.0 MHZ	13 26
	UIDE_DIOW_L	L:S::400 MIL			(200)			100.0 MHZ	13 26
	UIDE_DIOR_L	L:S::600 MIL		10 MIL SPACING	(200)			100.0 MHZ	13 26
	UIDE_DMACK_L	L:S::400 MIL			(200)			100.0 MHZ	13 26
	UIDE_CS0_L	L:S::500 MIL			(200)			100.0 MHZ	13 26
	UIDE_CS1_L	L:S::500 MIL			(200)			100.0 MHZ	13 26
	UIDE_DMARQ	L:S::400 MIL			(200)			100.0 MHZ	13
	UIDE_IOCHRDY	L:S::600 MIL		10 MIL SPACING	(200)			100.0 MHZ	13 26
	UIDE_INTRQ	L:S::400 MIL			(200)			100.0 MHZ	13
	HD_DATA<15..0>	L:S:5000:6500			(200)			100 MHZ	26
	HD_ADDR<2..0>	L:S:5000:6500	7		(200)			100 MHZ	26
	HD_RESET_L	L:S:4000 MIL:6000 MIL	4		(200)	TOTAL UIDE+HD SKEW <500MIL		100.0 MHZ	26
	HD_DIOW_L	L:S:3000 MIL:5200 MIL	4		(200)			100.0 MHZ	26
	HD_DIOR_L	L:S:6100 MIL:6150 MIL	4	10 MIL SPACING	(200)			100.0 MHZ	26
	HD_DMACK_L	L:S:4500 MIL:6000 MIL	4		(200)			100.0 MHZ	26
	HD_CS0_L	L:S:3000 MIL:6000 MIL	4		(200)			100.0 MHZ	26
	HD_CS1_L	L:S:3000 MIL:6000 MIL	4		(200)			100.0 MHZ	26
	HD_DMARQ	L:S:4500 MIL:6000 MIL	4		(200)			100.0 MHZ	13 26
	HD_IOCHRDY	L:S:6200 MIL:6300 MIL	4	10 MIL SPACING	(200)			100.0 MHZ	26
	HD_INTRQ	L:S:3000 MIL:5000 MIL	4					100.0 MHZ	13 26
EIDE INTREPID	EIDE_DATA<15..0>	L:S::850						33 MHZ	13 26
	EIDE_ADDR<2..0>	L:S::850						33 MHZ	13 26
	EIDE_CS0_L	L:S::850 MIL						33.00 MHZ	13 26
	EIDE_CS1_L	L:S::850 MIL						33.00 MHZ	13 26
	EIDE_RD_L	L:S::500 MIL						33.00 MHZ	13 26
	EIDE_WR_L	L:S::500 MIL						33.00 MHZ	13 26
	EIDE_IOCHRDY	L:S::500 MIL						33.00 MHZ	13 26
	EIDE_INT	L:S::500 MIL						33.00 MHZ	13 26
	EIDE_RST_L	L:S::500 MIL						33.00 MHZ	13 26
	EIDE_DMACK_L	L:S::500 MIL						33.00 MHZ	13 26
	EIDE_DMARQ	L:S::500 MIL						33.00 MHZ	13 26
OPTICAL	EIDE_OPTICAL_DATA<15..0>	L:S:4000:6000						33 MHZ	26 41
	EIDE_OPTICAL_ADDR<2..0>	L:S:4000:6000						33 MHZ	26 41
	EIDE_OPTICAL_CS0_L	L:S:4500 MIL:6500 MIL						33.00 MHZ	26 41
	EIDE_OPTICAL_CS1_L	L:S:4500 MIL:6500 MIL						33.00 MHZ	26 41
	EIDE_OPTICAL_READ_L	L:S:4500 MIL:6500 MIL						33.00 MHZ	26 41
	EIDE_OPTICAL_WR_L	L:S:4500 MIL:6500 MIL						33.00 MHZ	26 41
	EIDE_OPTICAL_IOCHRDY	L:S:4500 MIL:6500 MIL						33.00 MHZ	26 41
	EIDE_OPTICAL_INT	L:S:5000 MIL:7000 MIL						33.00 MHZ	26 41
	EIDE_OPTICAL_RST_L	L:S:4500 MIL:6500 MIL						33.00 MHZ	26 41
	EIDE_OPTICAL_DMAACK_L	L:S:4500 MIL:6500 MIL						33.00 MHZ	26 41
	EIDE_OPTICAL_DMA_RQ	L:S:4500 MIL:6500 MIL						33.00 MHZ	26 41
ETHERNET MII	ENET_LINK_RXD<7..0>	L:S:8000:9000	7	(400)		(400)			13 28
	ENET_RX_DV	L:S:8000 MIL:9000 MIL							13 28
	ENET_RX_ER	L:S:8000 MIL:9000 MIL							13 28
	ENET_PHY_TXD<7..0>	L:S:8000:9000	7	(400)		(400)			13 28
	ENET_LINK_TXD<7..0>	L:S::600							13
	ENET_PHY_TX_ER	L:S:8000 MIL:9000 MIL	4						13 28
	ENET_LINK_TX_ER	L:S::400 MIL							13
	ENET_PHY_TX_EN	L:S:8000 MIL:9000 MIL	4						13 28
	ENET_LINK_TX_EN	L:S::400 MIL							13
	ENET_MDIO	L:S:8000 MIL:9000 MIL							13 28
	ENET_MDC	L:S:8000 MIL:9000 MIL							13 28
	ENET_COL	L:S:8000 MIL:9000 MIL							13 28
	ENET_CRS	L:S:8000 MIL:9000 MIL							13 28
FIREWIRE MII	FW_LINK_DATA<7..0>	L:S:2700:3500	7	(400)		(400)			13 29
	FW_PHY_DATA<7..0>	L:S:4700:5500	7	(400)		(400)			29
	FW_LINK_CNTL<1..0>	L:S:9000:10000							13 29
	FW_PHY_CNTL<1..0>	L:S::300							29
	FW_LINK_LREQ	L:S::300 MIL							13
	FW_PHY_LREQ	L:S:8500 MIL:9500 MIL							13 29
	FW_PINT	L:S:8500 MIL:9500 MIL							13 29

PRIORITY: 4
PRIMARY LAYERS: 9
SECONDARY LAYERS: 4,7
GOAL: MINIMIZE TH VIAS

PRIORITY: 7
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 6
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 8
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 5
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 5
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR	RELATIVE_PROPAGATION_DELAY	MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	MAX_VIAS	
FIREWIRE Zo = 110	124 FW_TPI0N	FW_TPI0	FW_TPI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING		29 30 41
	124 FW_TPI0P	FW_TPI0	FW_TPI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING		29 30 41
	124 FW_TPO0N	FW_TPO0	FW_TPO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING		29 30 41
	124 FW_TPO0P	FW_TPO0	FW_TPO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING		29 30 41
	FW_TPBI0N	FW_TPBI0	FW_TPBI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING		30
	FW_TPBI0P	FW_TPBI0	FW_TPBI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING		30
	FW_TPAO0N	FW_TPAO0	FW_TPAO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING		30
	FW_TPAO0P	FW_TPAO0	FW_TPAO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING		30
	FW_TPA1N	FW_TPA1	FW_TPA1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING		29 30
	FW_TPA1P	FW_TPA1	FW_TPA1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING		29 30
	FW_TPB1N	FW_TPB1	FW_TPB1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING		29 30
	FW_TPB1P	FW_TPB1	FW_TPB1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING		29 30
	FW_TPI1N	FW_TPI1	FW_TPI1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING		30 41
	FW_TPI1P	FW_TPI1	FW_TPI1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING		30 41
	FW_TPO1N	FW_TPO1	FW_TPO1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING		30 41
	FW_TPO1P	FW_TPO1	FW_TPO1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING		30 41
ETHERNET Zo = 100	MDI_P<0>	ENET_MDI0	ENET_MDI0:G:U43.29:J23.1:0 MIL:100 MIL		ENET 11 MIL SPACING ENET 11 MIL SPACING		28 41
	MDI_M<0>	ENET_MDI0	ENET_MDI0:G:U43.31:J23.2:0 MIL:100 MIL		ENET 11 MIL SPACING ENET 11 MIL SPACING		28 41
	MDI_P<1>	ENET_MDI1	ENET_MDI1:G:U43.33:J23.3:0 MIL:100 MIL		ENET 11 MIL SPACING ENET 11 MIL SPACING		28 41
	MDI_M<1>	ENET_MDI1	ENET_MDI1:G:U43.34:J23.4:0 MIL:100 MIL		ENET 11 MIL SPACING ENET 11 MIL SPACING		28 41
	MDI_P<2>	ENET_MDI2	ENET_MDI2:G:U43.39:J23.7:0 MIL:100 MIL		ENET 11 MIL SPACING ENET 11 MIL SPACING		28 41
	MDI_M<2>	ENET_MDI2	ENET_MDI2:G:U43.41:J23.8:0 MIL:100 MIL		ENET 11 MIL SPACING ENET 11 MIL SPACING		28 41
	MDI_P<3>	ENET_MDI3	ENET_MDI3:G:U43.42:J23.9:0 MIL:100 MIL		ENET 11 MIL SPACING ENET 11 MIL SPACING		28 41
	MDI_M<3>	ENET_MDI3	ENET_MDI3:G:U43.43:J23.10:0 MIL:100 MIL		ENET 11 MIL SPACING ENET 11 MIL SPACING		28 41
LVDS Zo = 100 LOWER	CLKLVDS_LN	CLKLVDS_L	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING 100 OHM SPACING	4	21 23 41
	CLKLVDS_LP	CLKLVDS_L	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING 100 OHM SPACING	4	21 23 41
	LVDS_L0N	LVDS_L0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING 100 OHM SPACING		21 23 41
	LVDS_L0P	LVDS_L0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING 100 OHM SPACING		21 23 41
	LVDS_L1N	LVDS_L1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING 100 OHM SPACING		21 23 41
	LVDS_L1P	LVDS_L1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING 100 OHM SPACING		21 23 41
	LVDS_L2N	LVDS_L2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING 100 OHM SPACING		21 23 41
	LVDS_L2P	LVDS_L2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING 100 OHM SPACING		21 23 41
UPPER	CLKLVDS_UN	CLKLVDS_U	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING 100 OHM SPACING	4	
	CLKLVDS_UP	CLKLVDS_U	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING 100 OHM SPACING	4	
	LVDS_U0N	LVDS_U0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING 100 OHM SPACING		
	LVDS_U0P	LVDS_U0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING 100 OHM SPACING		
	LVDS_U1N	LVDS_U1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING 100 OHM SPACING		
	LVDS_U1P	LVDS_U1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING 100 OHM SPACING		
	LVDS_U2N	LVDS_U2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING 100 OHM SPACING		
	LVDS_U2P	LVDS_U2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING 100 OHM SPACING		
TMDS Zo = 100	TMDS_CLKN	CLKTMDS	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING 100 OHM SPACING	5	20 23
	TMDS_CLKP	CLKTMDS	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING 100 OHM SPACING	5	20 23
	TMDS_DN<0>	TMDS_D0		500.0000	100 OHM SPACING 100 OHM SPACING	8	20 23 41
	TMDS_DP<0>	TMDS_D0		500.0000	100 OHM SPACING 100 OHM SPACING	8	20 23 41
	TMDS_DN<1>	TMDS_D1		500.0000	100 OHM SPACING 100 OHM SPACING	8	20 23 41
	TMDS_DP<1>	TMDS_D1		500.0000	100 OHM SPACING 100 OHM SPACING	8	20 23 41
	TMDS_DN<2>	TMDS_D2		500.0000	100 OHM SPACING 100 OHM SPACING	8	20 23 41
	TMDS_DP<2>	TMDS_D2		500.0000	100 OHM SPACING 100 OHM SPACING	8	20 23 41
	128 ATI_TMDS_CLKN	ATI_CLKTMDS	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING 100 OHM SPACING	5	20 21
	128 ATI_TMDS_CLKP	ATI_CLKTMDS	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING 100 OHM SPACING	5	20 21
	128 ATI_TMDS_DN<0>	ATI_TMDS_D0		200.0000	100 OHM SPACING 100 OHM SPACING	8	20 21
	128 ATI_TMDS_DP<0>	ATI_TMDS_D0		200.0000	100 OHM SPACING 100 OHM SPACING	8	20 21
	128 ATI_TMDS_DN<1>	ATI_TMDS_D1		200.0000	100 OHM SPACING 100 OHM SPACING	8	20 21
	128 ATI_TMDS_DP<1>	ATI_TMDS_D1		200.0000	100 OHM SPACING 100 OHM SPACING	8	20 21
	128 ATI_TMDS_DN<2>	ATI_TMDS_D2		500.0000	100 OHM SPACING 100 OHM SPACING	8	20 21
	128 ATI_TMDS_DP<2>	ATI_TMDS_D2		500.0000	100 OHM SPACING 100 OHM SPACING	8	20 21
USB 1.1 Zo = 90	USB_DEM	USB_DE	USB_DE:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING		14
	USB_DEP	USB_DE	USB_DE:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING		14
	USB_DFM	USB_DF	USB_DF:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING		14
	USB_DFP	USB_DF	USB_DF:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING		14
	BT_USB_DM	BT_USB_D	BT_USB:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING		14 27 41
	BT_USB_DP	BT_USB_D	BT_USB:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING		14 27 41
	USB_TPAD_N	USB_TPAD_N	TPAD_USB:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING		14 24 41
	USB_TPAD_P	USB_TPAD_P	TPAD_USB:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING		14 24 41
USB 2.0 Zo = 90	NEC_USB_DAM	USB_D1	USB_D1:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING		17 27 41
	NEC_USB_DAP	USB_D1	USB_D1:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING		17 27 41
	NEC_USB_DBM	USB_D2	USB_D2:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING		17 27 41
	NEC_USB_DBP	USB_D2	USB_D2:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING		17 27 41
THERMOSTAT	THERM1_DM		THERM1:G:L:S:0 MIL:100 MIL				27
	THERM1_DP		THERM1:G:L:S:0 MIL:100 MIL				27
	THERM2_DM		THERM2:G:L:S:0 MIL:100 MIL				27
	THERM2_DP		THERM2:G:L:S:0 MIL:100 MIL				27
	REMOVE CONSTRAIN TO AVOID DRC OCCUR						
	1772_CSSN						32
	1772_CSSP						32
	1772_CSIN						32
	1772_CSIP						32
	3V_SNSM						34
	3V_SNSP						34
	5V_SNSM						34
	5V_SNSP						34
	THERM1_M_DM						27
	THERM1_M_DP						27
	THERM2_M_DM						27
	THERM2_M_DP						27
	THERM1_A_DM						27
	THERM1_A_DP						27
	THERM2_A_DM						27
	THERM2_A_DP						27

PRIORITY: 3
PRIMARY LAYERS: 4,7 FOR CONTROLLED IMPEDANCE DIFF PAIRS
SECONDARY LAYERS: 2,9 FOR UNCONTROLLED IMPEDANCE DIFF PAIRS

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3MIL (TRACE WIDTH)
S = 11MIL (TRACE SEPERATION)
H = 16.8MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 106.2 OHMS
Zo(single) = 55.4 OHMS

Clear adjacent power plane!
Zo will be lower due to asymmetric stackup.

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3.1MIL (TRACE WIDTH)
S = 4.9MIL (TRACE SEPERATION)
H = 9.6MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 94 OHMS
Zo(single) = 50 OHMS

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3.9MIL (TRACE WIDTH)
S = 5.6MIL (TRACE SEPERATION)
H = 9.6MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 89.8 OHMS
Zo(single) = 46.6 OHMS

LAYERS 2 OR 9

SIGNAL CONSTRAINTS - PAGE 2

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	B
SCALE NONE	SHT 39 OF 46	

POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
MAIN/SLEEP	+24V_PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	41
	+BATT	VOLTAGE=12.8V	MIN_LINE_WIDTH=10MIL	MIN_NECK_WIDTH=25MIL	
	+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	41
	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	41
	+5V_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	41
	+3V_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24 41
	+3V_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	41
	+3V_PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	41
	+2_5V_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	41
	+2_5V_SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_8V_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	41
	+1_8V_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP_VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
ADAPTER	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	32 33 41
	1436 +ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	32 40
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	32 40
	+ADAPTER_SENSE	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	32
BATTERY CHARGER	+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32 41
	BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32 41
	1772_DCIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		32
	1772_LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+BATT_14V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+BATT_24V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+BATT_RSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	32
	1772_LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		32
	1772_DLOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		32
	1772_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10		32
PMU	+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10		33
	+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10		33
	+4_85V_RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		31 33
	+4_6V_BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10		33 34
	+4_85V_ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		33
	+3V_PMU_ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		33
	+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		27 31
MISC HD	+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26 34
	+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
TRACKPAD	+5V_TPAD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=10		41
HALL EFFECT	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		24 41
VIDEO	+14V_INV	VOLTAGE=14V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23 41
	+5V_INV_UF_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23
	+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23 41
	+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	23 41
	+5V_DDC_SLEEP_UF	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	23
	+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10	23 41
	+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23
	GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		23
	GPU_TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		23
	TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		23 41
	TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		23 41
AUDIO	1435 +5V_MAIN_AUD	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27 34
	1435 +3V_MAIN_AUD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27 34
	1435 AUD_GND	VOLTAGE=0V	MIN_LINE_WIDTH=50		27
FAN	1438 +FAN_PWR	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27 41
	FAN1_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	41
	FAN2_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	41

I/O AREA		VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	IN
INVERTER	CHGND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN
TRACKPAD	CHGND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN
LVDS	CHGND3	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN
	CHGND4	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN

ENET_CTAP_CHGND		VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
CPU	CPU_VCORE_SLEEP	VOLTAGE=1.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 6 35 41
	CPU_AVDD	VOLTAGE=1.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
	MAXBUS_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 6 7 8 15 16 35
	1436 CPU_AVDD_VIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
	1436 CPU_AVDD_VOUT	VOLTAGE=1.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
DDR RAM	DDR_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		11
INTREPID	1435 +2_5V_INTREPID	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	9 10 15 16
	+3V_INTREPID_USB	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	14
PLLS	+1_5V_INTREPID_PLL	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	8 12 14
	+1_5V_INTREPID_PLL1	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL2	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL3	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL4	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL5	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	12
	+1_5V_INTREPID_PLL6	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	12
	+1_5V_INTREPID_PLL7	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	8
	+1_5V_INTREPID_PLL8	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
REFERENCE	INT_MEM_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		9
	INT_AGP_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		12 19
	INT_MEM_REF_H	VOLTAGE=0V	MIN_LINE_WIDTH=10		9
	VIDE_REF	VOLTAGE=0V	MIN_LINE_WIDTH=8		13
AIRPORT	+3V_AIRPORT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	41
CARDBUS	1436 +3V_SLEEP_PCCARD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18
	+VCC_CBUS_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18
	+VPP_CBUS_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18
ATI M11	GPU_VCORE	VOLTAGE=1.2V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	19 21 41
	+3V_GPU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 19 21 22
	+3V_GPU_FLT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	+2_5V_GPU	VOLTAGE=2.5V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	22
	GPU_MEM_IO	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	19 22
	GPU_MEM_IO_FLT	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	+2_5V_GPU_MEMCORE	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	+1_8V_GPU	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	19 20 21 22
	+1_5V_AGP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 15 16 19 21 22
	+2_5V_GPU_PNLIO	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	22
	+1_8V_ATI_PVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21 22
	+1_5V_AGP_GPU	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	22
	+1_5V_GPU_VDD15	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
	+1_8V_GPU_VDDDI	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
	GPU_VCORE_VDDCI	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	+2_5V_GPU_A2VDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
	+1_8V_GPU_AVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
	+1_8V_GPU_PNLPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
	+1_8V_GPU_PNLIO	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
	+2_5V_GPU_MCLK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	22
	+1_8V_GPU_AVDDQ	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	22
	+1_8V_GPU_MEMPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	22
	+3V_ATI_OSC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	+3V_ATI_SS	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	1436 +GPU_VDD15_UF	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	1434 +2_5V_SLEEP_NECK1	VOLTAGE=2.5V	MIN_LINE_WIDTH=10		21
	1436 +3V_SLEEP_NECK	VOLTAGE=3V	MIN_LINE_WIDTH=10		36
	1436 +1_5V_AGP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		21
	1436 +1_8V_PVDD_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		21
	1436 GPU_VCORE_NECK	VOLTAGE=1.2V	MIN_LINE_WIDTH=10		21
	1436 +GPU_VDD15_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		21
	1436 +2_5V_SLEEP_NECK2	VOLTAGE=2.5V	MIN_LINE_WIDTH=10		36
	1436 +1_8V_SLEEP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		36
	1436 +1_5V_SLEEP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		36
	1436 +1_8V_ATI_TPVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	22
	1436 +1_8V_GPU_TP_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
ETHERNET 88E1111	+2_5V_MARVELL	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+2_5V_MARVELL_AVDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_0V_MARVELL	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	LTC3405_SW	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
NEC USB2.0	1436 +3V_NEC_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	17
	1436 NEC_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	17
FW	1436 LM2594_IN	VOLTAGE=33V	MIN_LINE_WIDTH=40	MIN_NECK_WIDTH=12	29
	1436 +FW_PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	30
	1436 +FW_SW	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	30
	1436 +FW_AMP_SENSE	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	
	+FW_PWR_OR	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29 30
	1436 +FW_PWR1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	30
	+FW_VP0	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	30 41
	+FW_VP1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	30 41
	+3V_FW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29 30
	+3V_FW_UF	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+3V_FW_AVDD_PORT2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+3V_FW_AVDD_PORT1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+3V_FW_AVDD_PORT0	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+3V_FW_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+1_95V_FW_DVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+1_95V_FW_DVDD_RX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+1_95V_FW_DVDD_TX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+1_95V_FW_DVDD_PORT1	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+1_95V_FW_PLLVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+1_95V_FW_PLL400VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+1_95V_FW_PLL500VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	FW_VGND0	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	30
	1436 FW_VGND1	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	30
	1436 FW_VDD_ON	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
LTC1625 14V SWITCHER	1625_VIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		33
	1625_VSW	VOLTAGE=14V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	+PBUS_JUMPER	VOLTAGE=14V	MIN_LINE_WIDTH=10		33
	1625_EXTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		33
	1625_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		33
	1625_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		33
	1V20_REF	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	32 33
LTC3707 5V SWITCHER	3707_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	34
	5V_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	34
	5V_RSNS	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	34
	+5V_MAIN_JUMPER	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	34
3V SWITCHER	3V_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	34
	3V_RSNS	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	34
	+3V_MAIN_JUMPER	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	34
	3707_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		34
MAX1715 2.5V SWITCHER	2_5V_LX	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	36
	2_5V_LX_F	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	36
	2_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	36
	2_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	36
	2_5V_DH	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	36
	2_5V_DL	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	36
1.65V SWITCHER	1_5V_FB	VOLTAGE=1.5V	MIN_LINE_WIDTH=8		36
	1_5V_LX	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	36
	1_5V_LX_F	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	36
	1_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	36
	1_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	36
	1_5V_DH	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	36
	1_5V_DL	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	36
CONTROL	1_5V_ILIM		MIN_LINE_WIDTH=8		36
	2_5V_ILIM		MIN_LINE_WIDTH=8		36
	MAX1715_TON		MIN_LINE_WIDTH=8		36
	MAX1715_SKIP		MIN_LINE_WIDTH=8		36
	MAX1715_REF	VOLTAGE=2.0V	MIN_LINE_WIDTH=8		36
	MAX1715_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	36
	MAX1715_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	36
	VCORE_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
MAX1717	VCORE_LX	VOLTAGE=1.4V	MIN_LINE_WIDTH=200	MIN_NECK_WIDTH=10	35
	VCORE_DH		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	VCORE_DL		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	VCORE_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	VCORE_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	VCORE_ILIM		MIN_LINE_WIDTH=8		35
	VCORE_REF		MIN_LINE_WIDTH=8		35
	VCORE_TON	VOLTAGE=5V	MIN_LINE_WIDTH=8		35
	VCORE_CC		MIN_LINE_WIDTH=8		35
	VCORE_FB	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		35 41
	VCORE_TIME		MIN_LINE_WIDTH=8		35
	VCORE_VGATE		MIN_LINE_WIDTH=8		14 35
	VCORE_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30		35
	VCORE_GNDSNS	VOLTAGE=0V	MIN_LINE_WIDTH=8		35
	VCORE_SNS	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		35
	VCORE_GNDDIV	VOLTAGE=0V	MIN_LINE_WIDTH=8		35
	1437 VCORE_GNDA	VOLTAGE=0V	MIN_LINE_WIDTH=10		35
LTC1778	1778_VIN	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	1778_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	1778_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	21
	1778_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	1778_BST_RC	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	1778_TG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	1778_BG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	GPU_VCORE_SW	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	21
	GPU_VCORE_SW_F	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	21
	1778_ION		MIN_LINE_WIDTH=8		21
	1778_ITH		MIN_LINE_WIDTH=8		21
	1778_ITH_RC		MIN_LINE_WIDTH=8		21
	1778_VFB		MIN_LINE_WIDTH=8		21 41
	1778_FCB		MIN_LINE_WIDTH=8		21
	1778_VRNG		MIN_LINE_WIDTH=8		21
LTC3411	LTC3411_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	36
	LTC3411_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	36
	1_8V_SW	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	36
	1_8V_SW_F	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	36
	1_8V_VFB		MIN_LINE_WIDTH=8		36
	LTC3411_ITH_RC		MIN_LINE_WIDTH=8		36
	LTC3411_ITH		MIN_LINE_WIDTH=8		36
	LTC3411_SYNC		MIN_LINE_WIDTH=8		36
	LTC3411_SHDN		MIN_LINE_WIDTH=8		36
LTC1962 INT PLLS	LTC1962_INT_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	14
CY28512D LMU CONN	1436 +3V_MAIN_SSCG	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	1436 +3V_MAIN_LMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24
OPT DRIVER	1436 +5V_SLEEP_OPT	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26

SIGNAL CONSTRAINTS - PAGE 3

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SIZE	DRAWING NUMBER	REV.
D	051-6680	B
SCALE NONE	SHT 40 OF 46	

FUNCTIONAL TEST POINTS

PROBES ARE ON BOTTOM SIDE. MINIMUM PAD/HOLE SIZE IS 25 MIL.
FUNC_TEST IS ONLY PROPERTY USED BY THE TOOLS. FUNC_QTY IS FOR REFERENCE AND LISTS THE NUMBER OF TEST POINTS ON THAT NET AND WITHIN THAT GROUP/CONNECTOR.
FUNC_DIST IS SIMILARLY USED TO DEFINE MAXIMUM DISTANCE FROM A CONNECTOR.

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
SCAN/TEST	J2 JTAG_ASIC_TMS	TRUE			13 28
	J3 JTAG_ASIC_TDI	TRUE			13
	J1 JTAG_ASIC_TDO_TP	TRUE			28
	J4 JTAG_ASIC_TCK	TRUE			13 28
	J6 JTAG_ASIC_TRST_L	TRUE			13 28
	J5 CPU_CHKSTP_OUT_L	TRUE			5
	J7 CPU_SRESET_L	TRUE			5
	J9 CPU_HRESET_L	TRUE			5 6 7
	J8 JTAG_CPU_TMS	TRUE			5 6
	J10 JTAG_CPU_TDI	TRUE			5 6
	J12 JTAG_CPU_TDO_TP	TRUE			5
	J11 JTAG_CPU_TCK	TRUE			5 6
	J13 JTAG_CPU_TRST_L	TRUE			5 6
	J18 INT_JTAG_TEI	TRUE			13
	J20 INT_TST_MONIN_PD	TRUE			13
	J19 INT_TST_MONOUT_TP	TRUE			13
	J21 INT_TST_PLLEN_PD	TRUE			13
INT I2C	J15 INT_I2C_CLK0	TRUE			6 11 13 24
	J14 INT_I2C_DATA0	TRUE			6 11 13 24
	J16 INT_I2C_CLK1	TRUE			13 14 24 25 27
	J17 INT_I2C_DATA1	TRUE			13 14 24 25 27
PWR/GND	J21 +PBUS	TRUE			40
	J21 +24V_PBUS	TRUE			40
	J25 GPU_VCORE	TRUE			19 21 40
	J24 1778_VFB	TRUE			21 40
	J27 CPU_VCORE_SLEEP	TRUE			5 6 35 40
	J26 VCORE_FB	TRUE			35 40
	J21 +1_8V_MAIN	TRUE			40
	J21 +2_5V_MAIN	TRUE			40
	J219 +5V_MAIN	TRUE	2		40 41
	J220 +5V_SLEEP	TRUE	2		40 41
	J221 +3V_MAIN	TRUE	4		24 40
		TRUE		1000	IN
	J222 +3V_PMU	TRUE			40
CARDBUS	J36 CBUS_DET_1_L	TRUE		2000	18
	J35 CBUS_DET_2_L	TRUE		2000	18
DVI	J40 TMDS_CONN_CLKN	TRUE		1000	23 38
	J39 TMDS_CONN_CLKP	TRUE		1000	23 38
	J42 VGA_R	TRUE		1000	23
	J41 VGA_G	TRUE		1000	23
	J44 VGA_B	TRUE		1000	23
	J43 VGA_HSYNC	TRUE		1000	23
	J46 VGA_VSYNC	TRUE		1000	23
	J45 DVI_DDC_CLK_UF	TRUE		1000	23
	J47 DVI_DDC_DATA_UF	TRUE		1000	23
	J48 DVI_HPD_UF	TRUE		1000	23
	J49 +5V_DDC_SLEEP	TRUE		2000	23 40
		TRUE	2	2000	IN
CHGND1		TRUE	6	1000	IN
LVDS	J52 LVDS_L0N			1000	21 23 39
	J51 LVDS_L0P			1000	21 23 39
	J53 LVDS_L1N			1000	21 23 39
	J55 LVDS_L1P			1000	21 23 39
	J54 LVDS_L2N			1000	21 23 39
	J57 LVDS_L2P			1000	21 23 39
	J56 CLKLVDS_LN	TRUE		1000	21 23 39
	J58 CLKLVDS_LP	TRUE		1000	21 23 39
	J59 LVDS_DDC_CLK	TRUE		1000	21 23
	J60 LVDS_DDC_DATA	TRUE		1000	21 23
	J62 +3V_LCD	TRUE	2	2000	23 40
	J223 +3V_SLEEP	TRUE		2000	40 41
		TRUE	2	2000	IN
CHGND4		TRUE	6	1000	IN
INVERTER	J67 +14V_INV	TRUE		2000	23 40
	J66 +5V_INV_SW	TRUE		2000	23 40
	J68 BRIGHT_PWM	TRUE		2000	23
	J249 INV_GND	TRUE		2000	23
		TRUE		1000	IN
S-VIDEO	J70 TV_C	TRUE		2000	23
	J72 TV_Y	TRUE		2000	23
	J71 TV_COMP	TRUE		2000	23
	J73 TV_GND1	TRUE		2000	23 40
	J74 TV_GND2	TRUE		2000	23 40
LIO	J76 INT_I2S0_SND_TO_DAC	TRUE		1000	14 27
	J75 INT_I2S0_SND_LRCLK	TRUE		1000	14 27
	J78 INT_I2S0_SND_MCLK	TRUE		1000	14 27 37
	J83 INT_I2S0_SND_SCLK	TRUE		1000	14 27
	J82 INT_I2S0_SND_FROM_ADC	TRUE		1000	14 27
	J77 SND_HP_MUTE_L	TRUE		1000	14 27
	J79 SND_AMP_MUTE	TRUE		1000	27
	J84 SND_HW_RESET_L	TRUE		1000	14 27
	J85 SND_HP_SENSE_L	TRUE		1000	14 27
	J86 SND_LIN_SENSE_L	TRUE		1000	14 27
	J81 INT_I2C_CLK2	TRUE		1000	14 27
	J80 INT_I2C_DATA2	TRUE		1000	14 27
	J87 ADAPTER_DET	TRUE		1000	27 31
	J88 CHARGE_LED_L	TRUE		1000	27 31
	J89 NEC_LUSB_OCI_UF	TRUE		1000	17 27
	J90 NEC_LUSB_PPON	TRUE		1000	17 27
	J222 +5V_MAIN	TRUE	2	2000	40 41
	J221 +5V_SLEEP	TRUE	2	3000	40 41
	J220 +3V_SLEEP	TRUE		2000	40 41

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
USB	J194 NEC_USB_DAM	TRUE			17 27 39
	J195 NEC_USB_DAP	TRUE			17 27 39
	J196 NEC_USB_DBM	TRUE			17 27 39
	J197 NEC_USB_DBP	TRUE			17 27 39
	J198 BT_USB_DM	TRUE			14 27 39
	J199 BT_USB_DP	TRUE			14 27 39
	J100 USB_TPAD_N	TRUE			14 24 39
	J101 USB_TPAD_P	TRUE			14 24 39
RT. USB	J102 NEC_RUSB_PPON	TRUE			17 27
	J103 NEC_RUSB_OCI_UF	TRUE			17 27
WIRELESS	J104 PCI_AD<0..31>	TRUE		1000	9 12 17 18 26 39
	J105 PCI_FRAME_L	TRUE		1000	12 17 18 26 39
	J106 PCI_TRDY_L	TRUE		1000	12 17 18 26 39
	J107 PCI_IRDY_L	TRUE		1000	12 17 18 26 39
	J108 PCI_DEVSEL_L	TRUE		1000	12 17 18 26 39
	J109 PCI_STOP_L	TRUE		1000	12 17 18 26 39
	J110 PCI_PAR	TRUE		1000	12 17 18 26 39
	J111 AIRPORT_PCI_REQ_L	TRUE		1000	12 26
	J112 AIRPORT_PCI_GNT_L	TRUE		1000	12 26
	J113 AIRPORT_PCI_INT_L	TRUE		1000	14 26
	J114 MAIN_RESET_L	TRUE		1000	14 17 18 19 20 26 31
	J115 CLK33M_AIRPORT	TRUE		1000	12 26 37
	J116 PMU_PME_L	TRUE		1000	14 17 26 31
	J117 ROM_ONBOARD_CS_L	TRUE		1000	9
	J118 ROM_OE_L	TRUE		1000	9 12
	J119 ROM_CS_L	TRUE		1000	9 12
	J120 ROM_RW_L	TRUE		1000	9 12
	J229 RF_DISABLE_L	TRUE		1000	26
	J230 AIRPORT_CLKRUN_L	TRUE		1000	26
	J124 +3V_AIRPORT	TRUE	4	2000	40
		TRUE	6	1000	IN
OPTICAL	J125 EIDE_OPTICAL_DATA<0..15>	TRUE		2000	26 39
	J126 EIDE_OPTICAL_DMA_RQ	TRUE		2000	26 39
	J127 EIDE_OPTICAL_READ_L	TRUE		2000	26 39
	J128 EIDE_OPTICAL_DMAACK_L	TRUE		2000	26 39
	J129 EIDE_OPTICAL_ADDR<0..2>	TRUE		2000	26 39
	J130 EIDE_OPTICAL_CS0_L	TRUE		2000	26 39
	J131 EIDE_OPTICAL_CS1_L	TRUE		2000	26 39
	J132 EIDE_OPTICAL_RST_L	TRUE		2000	26 39
	J133 EIDE_OPTICAL_WR_L	TRUE		2000	26 39
	J134 EIDE_OPTICAL_IOCHRDY	TRUE		2000	26 39
	J135 EIDE_OPTICAL_INT	TRUE		2000	26 39
TRACKPAD	J136 +5V_TPAD_SLEEP	TRUE		3000	40
	J137 TPAD_F_TXD	TRUE		3000	
	J138 TPAD_F_RXD	TRUE		3000	
MODEM/ SERIAL	J139 SOFT_PWR_ON_L	TRUE		3000	23 24 31 35
	J140 COMM_RESET_L	TRUE		4000	14 27
	J141 COMM_SHUTDOWN	TRUE		4000	
	J142 COMM_RING_DET_L	TRUE		4000	14 27 31
	J143 COMM_TXD_L	TRUE		4000	14 27
	J144 COMM_TRXC	TRUE		4000	14 27
	J145 COMM_GPIO_L	TRUE		4000	14 27
	J146 COMM_DTR_L	TRUE		4000	14 27
	J147 COMM_RTS_L	TRUE		4000	14 27
	J148 COMM_RXD	TRUE		4000	14 27
KEYBOARD	J149 KBD_ID	TRUE		3000	24 31
	J150 KBD_INTL	TRUE		3000	
	J151 KBD_JIS	TRUE		3000	
	J152 KBD_CAPSLOCK_LED	TRUE		3000	
	J153 KBD_NUMLOCK_LED	TRUE		3000	
	J154 KBD_FUNCTION_L			3000	24 31
	J155 KBD_COMMAND_L			3000	24 31
	J156 KBD_OPTION_L			3000	24 31
	J157 KBD_CONTROL_L			3000	24 31
	J158 KBD_SHIFT_L			3000	24 31
	J159 KBD_X<0..9>			3000	24 31
	J160 KBD_Y<0..7>	TRUE		3000	
BATTERY	J161 +BATT_POS	TRUE	(100 MIL PROBE PREFERRED)	1000	32 40
	J162 BATT_NEG	TRUE	(100 MIL PROBE PREFERRED)	1000	32 40
	J163 BATT_CLK	TRUE		1000	32
	J164 BATT_DATA	TRUE		1000	32
	J165 PMU_BATT_DET_L	TRUE		1000	31 32
FANS	J166 +FAN_PWR	TRUE		3000	27 40
	J167 FAN1_TACH	TRUE		3000	27
	J168 FAN2_TACH	TRUE		3000	27
	J169 FAN1_GND	TRUE		3000	40
	J170 FAN2_GND	TRUE		3000	40
ETHERNET	J171 MDI_P<0..3>	TRUE		1000	28 39
	J172 MDI_M<0..3>	TRUE		1000	28 39
FIREWIRE	J173 FW_TPO0P	TRUE		1000	29 30 39
	J174 FW_TPO0N	TRUE		1000	29 30 39
	J175 FW_TPO0R	TRUE		1000	30
	J176 FW_TPI0P	TRUE		1000	29 30 39
	J177 FW_TPI0N	TRUE		1000	29 30 39
	J178 +FW_VP0	TRUE		1000	30 40
	J179 FW_VGND	TRUE		1000	41

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
FIREWIRE (CONT.)	J180 FW_TPO1P	TRUE		1000	30 39
	J181 FW_TPO1N	TRUE		1000	30 39
	J182 FW_TPI1P	TRUE		1000	30 39
	J183 FW_TPI1N	TRUE		1000	30 39
	J184 +FW_VP1	TRUE		1000	30 40
	J185 FW_VGND	TRUE		1000	41
DC PWR IN	J186 +ADAPTER	TRUE	3 (100 MIL PROBE PREFERRED)	1000	32 33 40
LMU/ALS	J250 ST7_SLEEP_LED_H	TRUE			24
	J250 PMU_SLEEP_LED	TRUE			24
	J250 PMU_LID_CLOSED_L	TRUE			24 31
	J250 LMU_DETECT	TRUE			24
		TRUE	6	1000	IN
			(100 MIL PROBE PREFERRED)		
MISC.	J190 SLEEP_LED	TRUE			24
	J191 PMU_KB_RESET_L	TRUE			
	J192 SLEEP	TRUE			24 27 31 34 36
	J193 PMU_CPU_HRESET_L	TRUE			6 31
	J194 BB_RESET_L	TRUE			6
	J224 +3V_PMU_RESET	TRUE			31 35
	J250 MMM_ACC_X_AXIS	TRUE			25
	J250 MMM_ACC_Y_AXIS	TRUE			25
	J250 MMM_ACC_Z_AXIS	TRUE			25
	J250 MMM_ACC_SELFTEST	TRUE			25
	J250 +BATT_ISNS_P	TRUE			25
	J250 +PPBATT_ISNS_N	TRUE			25
	J250 +PWR_SUPERCAP	TRUE			33
	REMOVE CONSTRAIN FOR UNUSED FUNCTIONAL TP				
	J248 +3V_HALL_EFFECT				24 40
	J248 LID_CLOSED_L				24
	J248 TMDS_DN<0..2>				20 23 39
	J248 TMDS_DP<0..2>				20 23 39

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6680	B
SCALE NONE	SHT 41 OF 46	

REVISION HISTORY

EVT2 RELEASE

08/13/04 - 1. CHANGE EXT TMDS SWING RESISTORS TO 510 OHM (R869, R876), REMOVE SI_RESET PULL HIGH
2. CHANGE RGB SIGNAL INPEDENCE (R341, R342, R346, R456, R458, R462)
3. ADD 2 RESISTORS (NO STUFF) BETWEEN FAN_PWM AND FAN_PWM_L OF FAN1 AND FAN2
4. CHANGE 2 CAPS (C233, C803) TO IMPROVE FEEDBACK PROTECTION AND PBUS CURRENT LIMIT CIRCUIT
5. MODIFY CPU_VCORE VID AND CPU_VCORE SETTING

08/16/04 - 1. MODIFY CPU_AVDD SETTING
08/20/04 - 1. ADD TRACKPAD POWER +5V_TPAD CONTROL CIRCUIT
09/01/04 - 1. CHANGE ALL FONTS INTO SMALL ONES
09/02/04 - 1. MODIFT CPU_VCORE VID AND CPU_VCORE SEETING AGAIN
2. MODIFY CPU_AVDD SEETING AGAIN
3. CHANGE INT TMDS DAMPING RESISTERS (R760-R767) TO 0 OHM
09/03/04 - 1. ADD MMM CIRCUIT, ARRANGE 2 INTREPID GPIOS FOR MM_FFIRQ_L, MM_SIRQ_L AND PULL UP RESISTORS R801, R802
2. ADD R803 BETWEEN DP6 AND DCDC_IN
3. ADD R804 AND SUPERCAP C692 ON +4_6V_BU
4. CHANGE TRACKPAD CONNECTOR J10 AND PIN OUT

09/06/04 - 1. ADD EMI SOLUTION L12
09/07/04 - 1. CHANGE TRACKPAD CONNECTOR PIN OUT
09/08/04 - 1. ADD BATTERY CURRENT SENSOR CIRCUIT
09/09/04 - 1. ADD EMI SOLUTION R816; ADD MMM RESET CIRCUIT
09/10/04 - 1. MODIFY FIREWIRE PORT0 POWER CIRCUIT
2. ADD NET FROM BATTERY CURRENT SENSOR CIRCUIT TO PMU
09/13/04 - 1. ADD CURRENT LIMITER R821 BETWEEN PMU(U29) AND U33
2. ADD PULL UP AND PULL DOWN RESISTORS FOR MMM SENSOR

DVT RELEASE

09/27/04 - 1. ADD ST MMM SENSOR CIRCUIT
10/14/04 - 2. ADD FIREWIRE POWER PROTECT CIRCUIT
10/15/04 - 3. CHANGE EXT_TMDS TERMINAL RESISTERS AND V SWINING RESISTOR
10/22/04 - 4. CHANGE FAN CONTROLLER FROM ADT7460 TO ADT7467
11/02/04 - 5. CHANGE BBANG IC TO ATTINY2313

PVT RELEASE

12/17/04 - 1. REMOVE ALL OPEN JUMPER
12/17/04 - 2. SCHEMATIC RELEASE FOR PRODUCTION

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SIZE	DRAWING NUMBER	REV.
D	051-6680	B
SCALE NONE	SHT 42 OF 46	

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*** Signal Cross-Reference for the entire design ***

+1_0V_MARVELL      28D2< 40B3>
+1_5V_AGP          12B5< 12D1< 12D4< 15D6< 16C8<
                   19C6< 19D6< 21A8< 21B4<> 21D5<>
                   22B8< 22D6< 40C3>
+1_5V_AGP_GPU      22C5< 40C3>
+1_5V_AGP_NECK     21B4<> 40B3>
+1_5V_GPU_VDD15    21D3< 40C3>
+1_5V_INTREPID_PLL  8D6< 12D4< 12D8< 14D6<> 40D3>
+1_5V_INTREPID_PLL1  14C3< 40D3>
+1_5V_INTREPID_PLL2  14D3< 40D3>
+1_5V_INTREPID_PLL3  14D3< 40D3>
+1_5V_INTREPID_PLL4  14D3< 40D3>
+1_5V_INTREPID_PLL5  12D3< 40D3>
+1_5V_INTREPID_PLL6  12D6< 40D3>
+1_5V_INTREPID_PLL7  8D5< 40D3>
+1_5V_INTREPID_PLL8  14D3< 40C3>
+1_5V_LDO          40D6>
+1_5V_MAIN         40D6>
+1_5V_SLEEP        40D6>
+1_5V_SLEEP_NECK   36D2<> 40B3>
+1_5V_SLEEP_VIN    40D6>
+1_8V_ATI_PVDD     21C5<> 22B6< 22B6< 22D6<> 40C3>
+1_8V_ATI_TPVDD    22D2<> 40B3>
+1_8V_GPU          19A8< 20A6< 21D7< 22A2< 22A6<
                   22B1< 22B6< 22C8< 22D6< 22D8< 40C3>
+1_8V_GPU_AVDD     22D5< 40B3>
+1_8V_GPU_AVDDQ    22D4< 22D7< 40B3>
+1_8V_GPU_DVO      22B2<
+1_8V_GPU_MEMPLL   22B5< 40B3>
+1_8V_GPU_PLL      22D5< 40C3>
+1_8V_GPU_PNLIO    22A5< 40B3>
+1_8V_GPU_PNLPLL   22B5< 40B3>
+1_8V_GPU_TP_PLL   22B5< 22D1< 40B3>
+1_8V_GPU_VDDDI    22C7< 22D4< 40C3>
+1_8V_MAIN         40D6> 41C6>
+1_8V_PVDD_NECK    21B5<> 40B3>
+1_8V_SLEEP        40D6>
+1_8V_SLEEP_NECK   36D2<> 40B3>
+1_95V_FW_DVDD     29C4< 29C7<> 29D5< 40A3>
+1_95V_FW_DVDD_PORT1  29D6< 40A3>
+1_95V_FW_DVDD_RX0  29C5< 40A3>
+1_95V_FW_DVDD_TX0  29C5< 40A3>
+1_95V_FW_PLL400VDD  29C4< 40A3>
+1_95V_FW_PLL500VDD  29D4< 40A3>
+1_95V_FW_PLLVDD   29D4< 29D6<> 40A3>
+2_5V_CG_MAIN      14C6<
+2_5V_GPU          22A7<> 40C3>
+2_5V_GPU_A2VDD    22D4< 22D7< 40B3>
+2_5V_GPU_MCLK     22C7< 22D4< 40B3>
+2_5V_GPU_MEMCORE  22C5< 40C3>
+2_5V_GPU_PNLIO    22A5< 40C3>
+2_5V_INTREPID     9A7< 10D3< 10D5< 10D6< 10D8< 15D6<
                   16B8< 40D3>
+2_5V_MAIN         40D6> 41C6>
+2_5V_MARVELL      28B8< 28C4< 40B3>
+2_5V_MARVELL_AVDD  28C4< 40B3>
+2_5V_MARVELL_CONN  28B3<>
+2_5V_REG          30A6<
+2_5V_REG_F        30A7<>
+2_5V_SLEEP        40D6>
+2_5V_SLEEP_NECK1  21C4<> 40B3>
+2_5V_SLEEP_NECK2  36D2<> 40B3>
+3V_AIRPORT        40C3> 41C3>
+3V_ATI_OSC_SLEEP  19B2< 40B3>
+3V_ATI_SS         19A3< 40B3>
+3V_CG_PLL_MAIN    14C6<
+3V_FW             29A3< 29D7<> 30B7<> 30D5< 40A3>
+3V_FW_AVDD        29C6< 40A3>
+3V_FW_AVDD_PORT0  29C6< 40A3>
+3V_FW_AVDD_PORT1  29C6< 40A3>
+3V_FW_AVDD_PORT2  29D6< 40A3>
+3V_FW_ESD         30A5< 30B4<> 30D3<>
+3V_FW_ESD_ILIM    30D4<
+3V_FW_ESD_R       30A6<
+3V_FW_UF          29D7<> 40A3>
+3V_GPU            12D1< 19B8< 19C6< 19C8< 19D6<
                   21C4< 21C5< 21C7< 21D7< 22A6< 22B1<
                   40C3>
+3V_GPU_FLT        22B2< 40C3>
+3V_HALL_EFFECT    24B2<> 40B6> 41C1>
+3V_INTREPID_USB   14C3< 40D3>
+3V_LCD            23B4<> 40B6> 41B6>
+3V_LCD_SW         23B4<> 40B6>
+3V_MAIN           24B8<> 40D6> 41C6>
+3V_MAIN_AUD       27C6<> 34C1<> 40B6>
+3V_MAIN_JUMPER    34D2<> 40D1>
+3V_MAIN_LMU       24D7<> 40A1>
+3V_MAIN_SSCG      40A1>
+3V_NEC_VDD        17B3< 17D7< 17D7< 40A3>
+3V_PMU            40D6> 41C6>
+3V_PMU_AVCC       27B1< 31B6< 31D5<> 40C6>
+3V_PMU_ESR        33A2< 40C6>
+3V_PMU_RESET      31C7< 35A4<> 41C1>
+3V_SENSOR         24B4<>
+3V_SLEEP          40D6> 41A6> 41B6>
+3V_SLEEP_NECK     36D1<> 40B3>
+3V_SLEEP_PCCARD   18D7<> 40C3>
+3V_SLP_OK_L       34B4<>
+3V_SLP_ON         34A5<>
+4_6V_BU           33B3<> 34B7< 40C6>
+4_85V_ESR         33A4< 40C6>
+4_85V_RAW         31A4< 33B4<> 40C6>
+5V_DDC_SLEEP      23D3<> 23D5<> 40B6> 41B6>
+5V_DDC_SLEEP_UF   23D6< 40B6>
+5V_HDD            26D1<>
+5V_HD_SLEEP       26D1<> 34A7<> 40C6>
+5V_INV_SW         23B2<> 40B6> 41A6>
+5V_INV_UF_SW      23B2<> 40B6>
+5V_MAIN           40D6> 41A6> 41C6>
+5V_MAIN_AUD       27C6<> 34C8<> 40B6>
+5V_MAIN_JUMPER    34D8<> 40D1>
+5V_SLEEP          40D6> 41A6> 41C6>
+5V_SLEEP_LMU      24C6<> 24C7<>
+5V_SLEEP_OPT      26B5<> 40A1>
+5V_TPAD           24B5<>
+5V_TPAD_FB        24B4<>
+5V_TPAD_SLEEP     40B6> 41B3>
+14V_INV           23B2<> 40B6> 41B6>
+24V_PBUS          40D6> 41C6>
+ADAPTER           32D8<> 33A7< 40C6> 41D1>
+ADAPTER_ILIM      33A6<> 40C6>
+ADAPTER_OR_BATT   33A5<> 40C6>
+ADAPTER_SENSE     32D4<> 40C6>
+ADAPTER_SW        32D5<> 40C6> 40C6>
+BATT              40D6>
+BATT_14V_FUSE     32D1<> 40C6>
+BATT_24V_FUSE     32B1< 32D2<> 40C6>
+BATT_ISNS_P       25A5<> 41C1>
+BATT_POS          32A4<> 40C6> 41A3>
+BATT_RSNS         32B2< 40C6>
+BATT_VSNS         32A4< 40C6>
+FAN_PWR           27A3< 27A4< 40B6> 41A3>
+FW_AMP_SENSE      40A3>
+FW_PBUS           30D7<> 40A3>
+FW_PWR1           30B5< 40A3>
+FW_PWR_CTRL       30A7<>
+FW_PWR_OR         29B8< 29D8<> 30D5<> 40A3>
+FW_PWR_OR_F       30B7<>
+FW_PWR_OR_GATE    30B8<>
+FW_PWR_OR_GATE_L  30A8<
+FW_SW             30D5<> 40A3>
+FW_VP0            30C1<> 40A3> 41A3>
+FW_VP1            30A3<> 40A3> 41D1>
+GPU_VDD15_NECK    21B5<> 40B3>
+GPU_VDD15_UF      21B5<> 21D4<> 40B3>
+HD_LOGIC_SLEEP    26C2<> 40C6>
+PBUS              40D6> 41C6>
+PBUS_JUMPER       33C3<> 40D1>
+PPBATT_ISNS_N     25A4<> 41C1>
+PWR_SUPERCAP      33A4< 41C1>
+VCC_CBUS_SW       18B1< 18B2< 18D2<> 40C3>
+VPP_CBUS_SW       18B1< 18B2< 18D2<> 40C3>
1V20_REF           32C7< 33C8< 40D1>
1V65_REF           32A5<
1_5V_BOOST         36C6<> 40C1>
1_5V_BST           36C5<> 40C1>
1_5V_DH            36C5<> 40C1>
1_5V_DL            36B5<> 40C1>
1_5V_FB            36B5< 36B7< 40C1>
1_5V_ILIM          36C5<> 40C1>
1_5V_LX            36B5<> 40C1>
1_5V_LX_F          36B7<> 36C5> 40C1>
1_5V_SLEEP_EN_L    36C7<> 36D7<>
1_8V_PVDD_STD      22D6<
1_8V_SLEEP_PWREN_L  36A3<>
1_8V_SW            36A5<> 40A1>

1_8V_SW_F          36A4<> 40A1>
1_8V_TPVDD_STD     22D1<
1_8V_VFB           36A5<> 40A1>
2_5V_BOOST         36C4<> 40D1>
2_5V_BST           36C4<> 40D1>
2_5V_DH            36C3<> 40D1>
2_5V_DL            36B3<> 40C1>
2_5V_FB            36B4<
2_5V_ILIM          36C5<> 40C1>
2_5V_LX            36B3<> 40D1>
2_5V_LX_F          36B2<> 36C4<> 40D1>
2_5V_SLEEP_PWREN_L  36C2<>
3V_5V_OK           24A6< 34B4<> 36A8< 36D6<
3V_5V_OK_G         24A6<
3V_5V_OK_L         24B5<>
3V_BG              34C4<>
3V_BOOST           34C4<>
3V_BOOST_ESR       34D3<>
3V_ITH             34C4<>
3V_ITH_RC          34C3<
3V_PMU_VTAP        33B3<
3V_RSNS            34D2< 40D1>
3V_RUNSS           34C4<
3V_SLEEP_PWREN_L   34B3<>
3V_SNSM            34C4< 39A2>
3V_SNSP            34C4< 39A2>
3V_SW              34C4<> 40D1>
3V_TG              34D4<>
3V_VOSNS           34C4<>
5V_BG              34C5<>
5V_BOOST           34C5<>
5V_BOOST_ESR       34D6<>
5V_HD_PWREN        34A8<>
5V_ITH             34C5<>
5V_ITH_RC          34C6<
5V_RSNS            34D7< 40D1>
5V_RUNSS           34C5<
5V_SLEEP_PWREN     34A8<>
5V_SNSM            34C5< 39A2>
5V_SNSP            34C5< 39A2>
5V_SW              34C5<> 40D1>
5V_TG              34C5<>
5V_VOSNS           34C5<>
1625_BG            33C5<>
1625_BST           33C5<
1625_BST_ESR       33C5<>
1625_COMP          32D2< 33C6<
1625_DIV           33C8<
1625_ENABLE        33D7<>
1625_ENABLE_L      33D6<>
1625_EXTVCC        33D5<> 40D1>
1625_FCB           33C6<
1625_INTVCC        33C5<> 40D1>
1625_RUNSS         33C6<
1625_SGND          33B7<> 40D1>
1625_TG            33C5<>
1625_VFB           33B5<>
1625_VIN           33C6< 40D1>
1625_VSW           33C4<> 40D1>
1772_ACIN          32B5<
1772_ACOK_L        32B5<> 32C4<>
1772_BST           32B4<>
1772_BST_ESR       32C3<
1772_CCI           32B5<>
1772_CCS           32B5<
1772_CCV           32B5<>
1772_CCV_RC        32B5<
1772_CELLS         32B4<
1772_CLS           32A4<
1772_CSIN          32B4<> 39A2>
1772_CSIP          32B4<> 39A2>
1772_CSSN          32C5< 39A2>
1772_CSSP          32C5< 39A2>
1772_DCIN          32B5< 40C6>
1772_DHI           32B4<>
1772_DLO           32B4<>
1772_DLOV          32B4<> 40C6>
1772_GND           32A5<> 40C6>
1772_ICHG          32B5<>
1772_ICTL          32B5<>
1772_IINP          32B5<
1772_LDO           32C4<> 40C6>
1772_LX            32B4<> 40C6>
1772_REF           32B5<>
1772_VCTL          32B5<
1778_BG            21A5<> 40B1>
1778_BST           21A5<> 40B1>
1778_BST_RC        21A5< 40B1>
1778_FCB           21A6< 40B1>
1778_GND           21A6< 21A7<> 40B1>
1778_ION           21A5< 40B1>
1778_ITH           21A6<> 40B1>
1778_ITH_RC        21A7< 40B1>
1778_SHDN_L        21A6<>
1778_TG            21A5<> 40B1>
1778_VCC           21A5< 40B1>
1778_VFB           21A2< 21A5< 40B1> 41C6>
1778_VIN           21A5< 40B1>
1778_VRNG          21A6< 40B1>
3405_MODE          28D5<
3405_VFB           28D4<>
3707_FCB           34C5<
3707_FSET          34C5<
3707_INTVCC        34D4<> 40D1>
3707_SGND          34B5<> 40D1>
3707_STBY          34C5<>
A29_CLS_ADJ        32A5<>
A29_CURRENT_ADJ    32C4<>
A29_DETECT         31A2< 32A5<> 32C4<>
A29_DET_L          31A3<
A29_DET_REF        31A4<
AC_DET             31A4<
AC_DIV             32C7<
AC_ENABLE_GATE     32D6<>
AC_ENABLE_L        32C5<>
AC_GTR_18V         32C3<>
AC_IN              28B8<> 30C8< 31B3< 32C5<> 32C6<>
AC_IN_FW_CNTL      30C7<>
AC_IN_L            31A8<> 32C2<> 32C6<>
AC_IN_L_RC         32C2<>
ADAPTER_DET        27D8<> 31A4< 41A6>
ADAPTER_I_REG      32D3<>
ADT7467_ADR_ENABLE_L  27B3<>
ADT7467_TACH3_TP  27B3<
ADT7467_THERM_L  24B4<> 27A2<> 27B3<
ADT7467_VCC        27C4<
ADT7467_VCORE_MON  5C8<> 27B4<
AGP8X_DET_PU       19C6<>
AGP_AD<0>          12D2<> 19C7<>
AGP_AD<15..0>      39D5>
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AGP_AD<2>          12C2<> 19C7<>
AGP_AD<3>          12C2<> 19C7<>
AGP_AD<4>          12C2<> 19C7<>
AGP_AD<5>          12C2<> 19C7<>
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AGP_AD<13>         12C2<> 19C7<>
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AGP_AD<17>         12C2<> 19C7<>
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AGP_AD<28>         12B2<> 19D7<>
AGP_AD<29>         12B2<> 19D7<>
AGP_AD<30>         12B2<> 19D7<>
AGP_AD<31>         12B2<> 19D7<>
AGP_AD_STB<0>      12A2<> 12B2< 19D6<> 39D5>
AGP_AD_STB<1>      12A2<> 12B2< 19D6<> 39D5>
AGP_AD_STB_L<0>    12A2<> 12B2< 19D6<> 39D5>
AGP_AD_STB_L<1>    12A2<> 12A2< 19D6<> 39D5>
AGP_ATI_INT_L      14B5<> 19B7<>
AGP_ATI_RESET_L    19B7<

AGP_ATI_VREF       19B7<
AGP_ATI_VREFG      19B7<
AGP_BUSY_L         12C4<> 12D2< 19D6>
AGP_CBE<0>         12B2<> 19B7<>
AGP_CBE<1..0>      39D5>
AGP_CBE<1>         12B2<> 19B7<>
AGP_CBE<2>         12B2<> 19B7<>
AGP_CBE<3..2>      39D5>
AGP_CBE<3>         12B2<> 19B7<>
AGP_DEVSEL_L       12B2<> 12C2< 19B7<> 39D5>
AGP_FRAME_L        12B2<> 12C2< 19B7<> 39D5>
AGP_GNT_L          12C2< 12D2<> 19B7< 39D5>
AGP_IRDY_L         12B2<> 12C2< 19B7<> 39D5>
AGP_PAR            12B2<> 19B7> 39D5>
AGP_PIPE_L         12A2<> 12B2<
AGP_RBF_L          12A2<> 12C2< 19C6> 39C5>
AGP_REQ_L          12C2< 12D2<> 19B7<> 39D5>
AGP_SBA<0>         12B2< 19C6>
AGP_SBA<7..0>      39D5>
AGP_SBA<1>         12B2<> 19C6>
AGP_SBA<2>         12B2<> 19C6>
AGP_SBA<3>         12B2<> 19C6>
AGP_SBA<4>         12B2<> 19C6>
AGP_SBA<5>         12B2<> 19C6>
AGP_SBA<6>         12B2<> 19C6>
AGP_SBA<7>         12B2<> 19C6<>
AGP_SB_STB         12B2<> 12B2< 19C6<> 39D5>
AGP_SB_STB_L       12A2< 12A2<> 19C6<> 39D5>
AGP_ST<0>          12A2<> 19C6<
AGP_ST<1>          12A2<> 19C6<
AGP_ST<2>          12A2<> 19C6<
AGP_STOP_L         12B2<> 12C2< 19B7<> 39D5>
AGP_STP_L          19C6<
AGP_SUS_STAT_L_PU  19C6<
AGP_TRDY_L         12B2<> 12C2< 19B7<> 39D5>
AGP_WBF_L          12A4<> 12B2< 19B7>
AIRPORT_CLKRUN_L  26C6<> 41C3>
AIRPORT_IDSEL      26C5<>
AIRPORT_PCI_GNT_L  12D7<> 26D5<> 41C3>
AIRPORT_PCI_INT_L  14B5<> 14D7< 26D5<> 41C3>
AIRPORT_PCI_REQ_L  12A7< 12D7<> 26D6<> 41C3>
ATI_AGP_FBSKEW<0>  21C2< 21C7<>
ATI_AGP_FBSKEW<1>  21C2< 21C7<>
ATI_BUS_CFG<0>     21B2< 21C7<>
ATI_BUS_CFG<1>     21B2< 21C7<>
ATI_BUS_CFG<2>     21B2< 21C7<>
ATI_CLK27M_IN      19A1< 21B7< 37B1>
ATI_CLK27M_OSC     19B2< 37B1>
ATI_CLK27M_OSC_SS  19A3< 19B1< 37B1>
ATI_DBI_HI_PU      19C6<>
ATI_DBI_LO_PU      19C6<>
ATI_DVOD<0>        20B8< 21D7<>
ATI_DVOD<23..0>    38C1>
ATI_DVOD<1>        20B8< 21D7<>
ATI_DVOD<2>        20B8< 21D7<>
ATI_DVOD<3>        20B8< 21D7<>
ATI_DVOD<4>        20B8< 21D7<>
ATI_DVOD<5>        20B8< 21D7<>
ATI_DVOD<6>        20B8< 21D7<>
ATI_DVOD<7>        20B8< 21D7<>
ATI_DVOD<8>        20B8< 21D7<>
ATI_DVOD<9>        20B8< 21D7<>
ATI_DVOD<10>       20B8< 21D7<>
ATI_DVOD<11>       20A8< 21D7<>
ATI_DVOD<12>       20B6< 21D7<>
ATI_DVOD<13>       20B6< 21D7<>
ATI_DVOD<14>       20B6< 21D7<>
ATI_DVOD<15>       20B6< 21D7<>
ATI_DVOD<16>       20B6< 21D7<>
ATI_DVOD<17>       20B6< 21D7<>
ATI_DVOD<18>       20B6< 21C7<>
ATI_DVOD<19>       20B6< 21C7<>
ATI_DVOD<20>       20B6< 21C7<>
ATI_DVOD<21>       20B6< 21C7<>
ATI_DVOD<22>       20B6< 21C7<>
ATI_DVOD<23>       20A6< 21C7<>
ATI_DVOD_DE        20A6< 20A8< 21C7<> 38C1>
ATI_DVOVMODE       22A3<
ATI_DVO_CLKP       19B4< 21C7<> 38C1>
ATI_DVO_HSYNC      20A8< 21C7<> 38C1>
ATI_DVO_VSYNC      20A6< 20A8< 21C7<> 38C1>
ATI_GPIO8_PD       21C7<>
ATI_GPIO9_SPN      21C7<>
ATI_GPIO10_SPN     21C7<>
ATI_GPIO11_SPN     21C7<>
ATI_GPIO12_SPN     21C7<>
ATI_GPIO13_SPN     21C7<>
ATI_HSYNC          21D5<> 23D8<
ATI_HSYNC_BUF      23D8<>
ATI_MEMTEST        19A6<>
ATI_MEMVMODE0      19A7<
ATI_MEMVMODE1      19A7<
ATI_OSC_OE         19B3<
ATI_PVDD_BYP       22D6<>
ATI_R2SET          21D6<>
ATI_RSET           21D6<>
ATI_RSTB_MSK       19C6<>
ATI_SSCLK_IN       19A2< 21B7<> 37B1>
ATI_SSCLK_UF       19A2<> 37B1>
ATI_TESTEN         21B7<
ATI_TMDS_CLKN      20C2< 21B7> 39B2>
ATI_TMDS_CLKP      20C2< 21B7> 39B2>
ATI_TMDS_DN<0>     20D2< 21B7> 39B2>
ATI_TMDS_DN<1>     20D2< 21B7> 39B2>
ATI_TMDS_DN<2>     20C2< 21B7> 39B2>
ATI_TMDS_DP<0>     20D2< 21B7> 39B2>
ATI_TMDS_DP<1>     20D2< 21B7> 39B2>
ATI_TMDS_DP<2>     20C2< 21B7> 39B2>
ATI_TPVDD_BYP      22D1<>
ATI_VSYNC          21D5<> 23D8<
ATI_VSYNC_BUF      23D8<>
ATI_X1CLK_SKEW<0>  21C2< 21C7<>
ATI_X1CLK_SKEW<1>  21B2< 21C7<>
AUD_GND            27C8<> 40B6>
AUXWIN_PU          21C6<>
BATTV_HIGH         32B7<>
BATTV_LOW          32B8<>
BATT_14PBUS_EN     32C1<>
BATT_14V_GATE      32C1<>
BATT_24PBUS_EN     32C2<>
BATT_24V_GATE      32C1<>
BATT_CLK           32A4<> 41A3>
BATT_DATA          32A4<> 41A3>
BATT_DIV           32A5<
BATT_ISNS_OUT      25A4<>
BATT_ISNS_R        25A3<>
BATT_LOW           32A6<>
BATT_LOW_L         32B6<>
BATT_NEG           32A4<> 40C6> 41A3>
BBANG_HRESET_L     6A2< 6B3<>
BBANG_JTAG_TCK     6A4< 6B2<> 6C2<
BBANG_TCK_EN       6A4<
BB_EEPR_ADDR0      6D3<
BB_EEPR_ADDR1      6D3<
BB_EEPR_ADDR2      6D3<
BB_EEPR_WP_PD      6D2<>
BB_MISO            6B3<> 6C2<
BB_MOSI            6B3<> 6C2<
BB_RESET_L         6C3< 41C1>
BB_SCK             6B3<> 6C2<
BFR_TDO            6C2< 6C2<>
BKFD_PROT_EN_L     32C5<>
BKFD_PROT_GATE     32D5<>
BRIGHT_PWM         23A2<> 41A6>
BRIGHT_PWM_UF      23A2<>
BT_USB_DM          14C1< 27D8<> 39B2> 41D3>
BT_USB_DP          14C1< 27D8<> 39B2> 41D3>
CBUS_ADDR<0>       18B1< 18B4>
CBUS_ADDR<1>       18B1< 18B4>
CBUS_ADDR<2>       18B1< 18B4>
CBUS_ADDR<3>       18B1< 18B4>
CBUS_ADDR<4>       18B1< 18B4>
CBUS_ADDR<5>       18B1< 18B4>
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CBUS_ADDR<7>       18B1< 18B4>
CBUS_ADDR<8>       18B1< 18B4>
CBUS_ADDR<9>       18B1< 18B4>
CBUS_ADDR<10>      18B4> 18C1<
CBUS_ADDR<11>      18B1< 18B4>
CBUS_ADDR<12>      18B1< 18B4>
CBUS_ADDR<13>      18B1< 18B4>
CBUS_ADDR<14>      18B1< 18B4>
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CBUS_ADDR<16>      18B1< 18B4<
CBUS_ADDR<17>      18B2< 18B4>
CBUS_ADDR<18>      18B2< 18B4>
CBUS_ADDR<19>      18B2< 18B4>
CBUS_ADDR<20>      18B2< 18B4>

CBUS_ADDR<21>      18B2< 18B4>
CBUS_ADDR<22>      18A4> 18B2<
CBUS_ADDR<23>      18A4> 18B2<
CBUS_ADDR<24>      18A4> 18B2<
CBUS_ADDR<25>      18A4> 18B2<
CBUS_ADDR_16_UF  18B5<>
CBUS_BVD1_L        18A2< 18C4<
CBUS_BVD2_L        18B2< 18C4<
CBUS_CE1_L         18C1< 18C4>
CBUS_CE2_L         18B2< 18B4>
CBUS_DATA<0>       18A1< 18A4<>
CBUS_DATA<1>       18A1< 18A4<>
CBUS_DATA<2>       18A1< 18A4<>
CBUS_DATA<3>       18A4<> 18C1<
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CBUS_DATA<7>       18A4<> 18C1<
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CBUS_DATA<9>       18A2< 18A4<>
CBUS_DATA<10>      18A2< 18A4<>
CBUS_DATA<11>      18A4<> 18C2<
CBUS_DATA<12>      18A4<> 18C2<
CBUS_DATA<13>      18A4<> 18C2<
CBUS_DATA<14>      18A4<> 18C2<
CBUS_DATA<15>      18A4<> 18C2<
CBUS_DET_1_L       18C2< 18C4< 41C6>
CBUS_DET_2_L       18A2< 18C4< 41C6>
CBUS_INPACK_L      18B2< 18B4<
CBUS_INT_L         14B5<> 14D7< 18A7<>
CBUS_IORD_L        18B2< 18C4>
CBUS_IOWR_L        18B2< 18C4>
CBUS_MFUNC1_PD     18A7< 18A7<>
CBUS_MFUNC2_PD     18A7< 18A7<>
CBUS_MFUNC3_PD     18A7< 18A7<>
CBUS_MFUNC4_PD     18A7< 18A7<>
CBUS_MFUNC5_PD     18A7< 18A7<>
CBUS_MFUNC6_PD     18A7< 18A7<>
CBUS_OE_L          18B1< 18C4>
CBUS_PCI_GNT_L     12D7<> 18A7<
CBUS_PCI_IDSEL     18B7<
CBUS_PCI_REQ_L     12A7< 12D7<> 18A7>
CBUS_PCI_RESET_L  18A7<
CBUS_READY         18B1< 18C4<
CBUS_REG_L         18B2< 18C4>
CBUS_RESET_L       18B2< 18C4>
CBUS_SUSPEND_PU  18A7< 18D7<
CBUS_VCCD0_L       18C4<>
CBUS_VCCD1_L       18C4<>
CBUS_VPPD0         18C4<>
CBUS_VPPD1         18C5<>
CBUS_VS1           18B2< 18C4<>
CBUS_VS2           18B2< 18C4<>
CBUS_WAIT_L        18B2< 18B4<
CBUS_WE_L          18B1< 18C4>
CBUS_WP_L          18A1< 18B4<
CG_ADDRSEL         14B7<
CG_CLKOUT          14B6<>
CG_FSEL            14B7< 14C5<
CG_FSEL_INT        14C5<>
CG_LOCK            14B7<>
CG_RESET_L         14B7<
CG_SYSCLK_EN       14B5< 14B7<
CHARGE_DISABLE     32A7<>
CHARGE_LED_L       27D8<> 31C6<> 31D7< 41A6>
CLK10M_PMU_XIN     31B6<
CLK10M_PMU_XOUT    31B6<
CLK10M_PMU_XOUT_UF  31B7<
CLK18M_INT_EXT     14B6<> 37B1>
CLK18M_INT_XIN     14A5< 37B1>
CLK18M_INT_XOUT    14A5<> 37B1>
CLK18M_XTAL_IN     14A5< 37B1>
CLK25M_ENET_XIN    28A7<>
CLK25M_ENET_XOUT   28A7<>
CLK25M_XTAL_IN     28A7<>
CLK32K_PMU_XIN     31B3<>
CLK32K_PMU_XOUT    31B3<>
CLK32K_PMU_XOUT_UF  31B2<>
CLK33M_AIRPORT     12D8< 26D5<> 37C1> 41C3>
CLK33M_AIRPORT_UF  12C7<> 37C1>
CLK33M_CBUS        12D8< 18A7< 37C1>
CLK33M_CBUS_UF     12C7<> 37C1>
CLK33M_NEC         12C8< 17B7< 37C1>
CLK33M_NEC_UF      12C7<> 37C1>
CLK66M_AGP_1_5V_TP  12C4>
CLK66M_GPU_AGP     12C8< 19B7< 37C1>
CLK66M_GPU_AGP_UF  12C7<> 37C1>
CLKENET_LINK_GBE_REF  13C5< 28C8< 37B1>
CLKENET_LINK_GTX  13C5<> 37A1>
CLKENET_LINK_RX  13D5< 28C8< 37B1>
CLKENET_LINK_TX  13D5< 28D8< 37A1>
CLKENET_PHY_GBE_REF  28C7<> 37B1>
CLKENET_PHY_GTX  13C6< 28C7< 37A1>
CLKENET_PHY_RX     28C7<> 37B1>
CLKENET_PHY_TX     28D7<> 37A1>
CLKFW_LINK_LCLK  13C3<> 37A1>
CLKFW_LINK_PCLK  13C3<> 29C3< 37A1>
CLKFW_PHY_LCLK     13C2< 29B7< 37A1>
CLKFW_PHY_PCLK     29B4> 29C4< 37A1>
CLKLVDS_LN         21B5> 23A4<> 39C2> 41B6>
CLKLVDS_LP         21B5> 23A4<> 39C2> 41B6>
CLKLVDS_UN         39C2>
CLKLVDS_UP         39C2>
COMM_DTR_L         14C2> 27C1<> 41B3>
COMM_GPIO_L        14C2<> 27C2<> 41B3>
COMM_RESET_L       14C5<> 27D3< 41B3>
COMM_RING_DET_L  14B5<> 14C7< 27D3< 31C6<> 41B3>
COMM_RTS_L         14C2> 27C1<> 41B3>
COMM_RXD           14C2<> 27C1<> 41B3>
COMM_SHUTDOWN      41B3>
COMM_TRXC          14C2<> 27C2<> 41B3>
COMM_TXD_L         14C2<> 27C2<> 41B3>
COMP_RC            33C6<
CPU_AACK_L         5A7< 8B5<> 8C2< 38D5>
CPU_ADDR<0>        5C7<> 8D5<>
CPU_ADDR<0..31>  38D5>
CPU_ADDR<1>        5C7<> 8D5<>
CPU_ADDR<2>        5C7<> 8D5<>
CPU_ADDR<3>        5C7<> 8D5<>
CPU_ADDR<4>        5C7<> 8D5<>
CPU_ADDR<5>        5C7<> 8C5<>
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CPU_ADDR<25>       5B7<> 8C5<>
CPU_ADDR<26>       5B7<> 8C5<>
CPU_ADDR<27>       5B7<> 8C5<>
CPU_ADDR<28>       5B7<> 8C5<>
CPU_ADDR<29>       5B7<> 8C5<>
CPU_ADDR<30>       5B7<> 8C5<>
CPU_ADDR<31>       5B7<> 8C5<>
CPU_ARTRY_L        5A7<> 8B5<> 8D2< 38D5>
CPU_AVDD           5C3< 40D3>
CPU_AVDD_ADJ       5C2<>
CPU_AVDD_SHDN_L  5C3<>
CPU_AVDD_VIN       5C3< 40D3>
CPU_AVDD_VOUT      5C2<> 40D3>
CPU_BG_L           5C7< 8C2< 8D5<> 38D5>
CPU_BR_L           5C7> 8D2< 8D5< 38D5>
CPU_BUS_VSEL       5C3< 7A6<
CPU_CHKSTP_OUT_L  5B3<> 5C2< 41D6>
CPU_CHKS_L         5A3< 5D2<
CPU_CI_L           5A7> 8B5<> 38D5>
CPU_CLKOUT_SPN     5C3>
CPU_CLK_EN         8A5< 31C4<>
CPU_DATA<0>        6D8<> 8D3<>
CPU_DATA<0..31>  38D5>
CPU_DATA<1>        6D8<> 8D3<>
CPU_DATA<2>        6D8<> 8D3<>
CPU_DATA<3>        6D8<> 8D3<>
CPU_DATA<4>        6D8<> 8D3<>
CPU_DATA<5>        6D8<> 8D3<>

CPU_DATA<6>        6D8<> 8D3<>
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CPU_DATA<8>        6D8<> 8D3<>
CPU_DATA<9>        6C8<> 8D3<>
CPU_DATA<10>       6C8<> 8D3<>
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CPU_DATA<26>       6C8<> 8C3<>
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CPU_DATA<30>       6C8<> 8C3<>
CPU_DATA<31>       6C8<> 8C3<>
CPU_DATA<32>       6C8<> 8C3<> 8D8<
CPU_DATA<32..63>  38D5>
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CPU_DATA<34>       6C8<> 8C3<> 8D8<
CPU_DATA<35>       6C8<> 8C3<> 8D8<
CPU_DATA<36>       6B8<> 8C3<> 8D8<
CPU_DATA<37>       6B8<> 8C3<> 8D8<
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CPU_DATA<39>       6B8<> 8B3<> 8D8<
CPU_DATA<40>       6B8<> 8B3<> 8C8<
CPU_DATA<41>       6B8<> 8B3<> 8C8<
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CPU_DATA<43>       6B8<> 8B3<> 8C8<
CPU_DATA<44>       6B8<> 8B3<> 8C8<
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CPU_DATA<47>       6B8<> 8B3<> 8B8<
CPU_DATA<48>       6B8<> 8A8< 8B3<>
CPU_DATA<49>       6B8<> 8A8< 8B3<>
CPU_DATA<50>       6B8<> 8A8< 8B3<>
CPU_DATA<51>       6B8<> 8A8< 8B3<>
CPU_DATA<52>       6B8<> 8A8< 8B3<>
CPU_DATA<53>       6B8<> 8A8< 8B3<>
CPU_DATA<54>       6B8<> 8A8< 8B3<>
CPU_DATA<55>       6B8<> 8A8< 8B3<>
CPU_DATA<56>       6B8<> 8B3< 8B3<>
CPU_DATA<57>       6B8<> 8B3< 8B3<>
CPU_DATA<58>       6B8<> 8B3< 8B3<>
CPU_DATA<59>       6B8<> 8B3< 8B3<>
CPU_DATA<60>       6B8<> 8B3< 8B3<>
CPU_DATA<61>       6B8<> 8B3< 8B3<>
CPU_DATA<62>       6A8<> 8B3< 8B3<>
CPU_DATA<63>       6A8<> 8B3< 8B3<>
CPU_DBG_L          5C3< 8A3<> 8C2< 38D5>
CPU_DRDY_L         5C3> 8A3< 8C2< 38D5>
CPU_DTI<0>         5C3< 8A3<>
CPU_DTI<0..2>      38D5>
CPU_DTI<1>         5C3< 8A3<>
CPU_DTI<2>         5C3< 8A3<>
CPU_EDTI           5A2< 5C3<
CPU_EMODE0_L       5A3< 7A4<
CPU_EMODE1_L       5A3< 5C2<
CPU_GBL_L          5A7<> 8B5<> 38D5>
CPU_HIT_L          5A7> 8B5< 8D2< 38D5>
CPU_HRESET_INV     7A7<>
CPU_HRESET_L       5B3< 5C2< 6A1<> 7A5< 7A8< 41D6>
CPU_L1TSTCLK       5B2< 5B3<
CPU_L2TSTCLK       5B3< 5C2<
CPU_LSSD_MODE      5B3< 5C2<
CPU_MCP_L          5B3< 5D2<
CPU_PLL_CFG<0>     5C3< 7D3<
CPU_PLL_CFG<1>     5C3< 7D3<
CPU_PLL_CFG<2>     5C3< 7D3<
CPU_PLL_CFG<3>     5C3< 7D3<
CPU_PLL_CFG<4>     5C3< 7D3<>
CPU_PLL_CFGEXT     7D4<>
CPU_PLL_FS00       7C4<>
CPU_PLL_FS01       7C4<
CPU_PLL_FS10       7C4<
CPU_PLL_STOP_BASE  7C7<
CPU_PLL_STOP_OC  7C4<> 7C8<> 31B6<>
CPU_PMONIN_L       5A3< 5C2<
CPU_PULLDOWN       5A2< 5A3< 5A3< 5C7<>
CPU_PULLUP         5A3< 5C2<
CPU_QACK_L         5B3< 8B5<> 38D5>
CPU_QREQ_L         5B3> 8B5< 8C2< 38D5>
CPU_SHD0_L         5A7<> 5D2<
CPU_SHD1_L         5A7<> 5D2<
CPU_SMI_L          5B3< 5C2< 31C4<>
CPU_SRESET_L       5B2< 5B3< 41D6>
CPU_SRWX_L         5A3< 5C2<
CPU_TA_L           5B3< 8A3<> 8D2< 38D5>
CPU_TBEN           5B3< 5D2< 8A5<>
CPU_TBST_L         5A7> 8B5<> 38D5>
CPU_TEA_L          5B3< 8A3<> 8C2< 38D5>
CPU_THERM_DM       6A6<> 27A6<
CPU_THERM_DP       6A6<> 27A6<
CPU_TSIZ<0>        5A7> 8B5<>
CPU_TSIZ<0..2>     38D5>
CPU_TSIZ<1>        5A7> 8B5<>
CPU_TSIZ<2>        5A7> 8B5<>
CPU_TS_L           5C7<> 8D2< 8D5<> 38D5>
CPU_TT<0>          5A7<> 8B5<>
CPU_TT<0..4>       38D5>
CPU_TT<1>          5A7<> 8B5<>
CPU_TT<2>          5A7<> 8B5<>
CPU_TT<3>          5A7<> 8B5<>
CPU_TT<4>          5A7<> 8B5<>
CPU_VCORE_HI_OC    7B8< 31D4<> 35C8<
CPU_VCORE_PWR_SEQ  35D8<>
CPU_VCORE_SEQ      35D8<
CPU_VCORE_SEQ_L    35D8<
CPU_VCORE_SLEEP    5D2< 5D8<> 6C6<> 35C1< 35D2< 40D3>
                   41C6>
CPU_VCORE_SNUB     35B3<
CPU_WT_L           5A7> 8B5<> 38C5>
CSLOT_ADDR3_SPN  13B7>
CSLOT_ADDR4_SPN  13B7>
CSLOT_ADDR5_SPN  13B7>
CSLOT_ADDR6_SPN  13B7>
CSLOT_ADDR7_SPN  13B7>
CSLOT_ADDR8_SPN  13B7>
CSLOT_ADDR9_SPN  13B7>
CSLOT_CE1_L_SPN  13C7>
CSLOT_CE2_L_SPN  13C7>
CSLOT_IORD_L_SPN  13C7>
CSLOT_IOWAIT_L_PU  13C7<
CSLOT_IOWR_L_SPN  13C7>
CSLOT_OE_L_SPN   13C7>
CSLOT_WE_L_SPN   13C7>
CURRENT_THRESHOLD  32C3<
CY25811_S0         19A3<
CY25811_S1         19A3<
DCDC_EN            21A7<> 30C8< 34B7<> 35C7<>
DCDC_EN_CTRL       30C7<>
DCDC_EN_L          34B6< 34B7<> 36C7<>
DDC_CLK_ISO        23D4<>
DDR_VREF           11D1< 11D3<> 11D5<> 11D6<> 11D8<>
                   40D3>
DVI_DDC_CLK        23D4<>
DVI_DDC_CLK_UF     23C5<> 23D3<> 41B6>
DVI_DDC_DATA       23C4<>
DVI_DDC_DATA_UF  23C5<> 41B6>
DVI_HPD            23C4<>
DVI_HPD_DIV        23C2<
DVI_HPD_UF         23C3< 23C5<> 41B6>
DVI_TURN_ON        23D3<>
DVI_TURN_ON_BASE  23D2<>
DVI_TURN_ON_ILIM  23D2<
EIDE_ADDR<0>       13B7> 26B8<
EIDE_ADDR<2..0>  39B5>
EIDE_ADDR<1>       13B7> 26B8<
EIDE_ADDR<2>       13B7> 26B8<
EIDE_CS0_L         13B7> 26B8< 39B5>
EIDE_CS1_L         13B7> 26A8< 39B5>
EIDE_DATA<0>       13C7<> 26C8<
EIDE_DATA<15..0>  39B5>
EIDE_DATA<1>       13C7<> 26C8<
EIDE_DATA<2>       13C7<> 26C8<
EIDE_DATA<3>       13C7<> 26C8<
EIDE_DATA<4>       13C7<> 26B8<
EIDE_DATA<5>       13B7<> 26B8<

EIDE_DATA<6>       13B7<> 26B8<
EIDE_DATA<7>       13B7<> 26B8<
EIDE_DATA<8>       13B7<> 26D8<
EIDE_DATA<9>       13B7<> 26C8<
EIDE_DATA<10>      13B7<> 26D8<
EIDE_DATA<11>      13B7<> 26C8<
EIDE_DATA<12>      13B7<> 26C8<
EIDE_DATA<13>      13B7<> 26C8<
EIDE_DATA<14>      13B7<> 26C8<
EIDE_DATA<15>      13B7<> 26C8<
EIDE_DMACK_L       13A7<> 26A8< 39B5>
EIDE_DMARQ         13A7< 26A8< 39B5>
EIDE_INT           13A7< 26A8< 39B5>
EIDE_IOCHRDY       13B7< 26A8< 39B5>
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EIDE_OPTICAL_ADDR<2..0>  39B5> 41C3>
EIDE_OPTICAL_ADDR<1>  26A5<> 26B7<
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EIDE_OPTICAL_CS0_L  26A5<> 26B7< 39B5> 41C3>
EIDE_OPTICAL_CS1_L  26A6<> 26A7< 39B5> 41C3>
EIDE_OPTICAL_DATA<0>  26A5<> 26C7<
EIDE_OPTICAL_DATA<15..0>  39B5> 41C3>
EIDE_OPTICAL_DATA<1>  26A5<> 26C7<
EIDE_OPTICAL_DATA<2>  26A5<> 26C7<
EIDE_OPTICAL_DATA<3>  26A5<> 26C7<
EIDE_OPTICAL_DATA<4>  26A5<> 26B7<
EIDE_OPTICAL_DATA<5>  26A5<> 26B7<
EIDE_OPTICAL_DATA<6>  26A5<> 26B7<
EIDE_OPTICAL_DATA<7>  26A5<> 26B7<
EIDE_OPTICAL_DATA<8>  26A6<> 26D7<
EIDE_OPTICAL_DATA<9>  26A6<> 26C7<
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EIDE_OPTICAL_DATA<13>  26A6<> 26C7<
EIDE_OPTICAL_DATA<14>  26A6<> 26C7<
EIDE_OPTICAL_DATA<15>  26A6<> 26C7<
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EIDE_OPTICAL_DMA_RQ  26A6<> 26A7< 39A5> 41C3>
EIDE_OPTICAL_INT  26A5<> 26A7< 39A5> 41B3>
EIDE_OPTICAL_IOCHRDY  26A5<> 26A7< 39A5> 41B3>
EIDE_OPTICAL_READ_L  26A6<> 26A7< 39B5> 41C3>
EIDE_OPTICAL_RST_L  26A7< 26B5<> 39A5> 41C3>
EIDE_OPTICAL_WR_L  26A5<> 26A7< 39B5> 41B3>
EIDE_RD_L          13A7> 26A8< 39B5>
EIDE_RST_L         13B7> 26A8< 39B5>
EIDE_WR_L          13A7> 26A8< 39B5>
ENET_COL           13C5< 28B7> 39A5>
ENET_COMA          28B7<>
ENET_CRS           13C5< 28B7> 39A5>
ENET_CTAP_CHGND  40A6>
ENET_ENERGY_DET  14B5<> 28B7<>
ENET_HSDACM        28A7<>
ENET_HSDACP        28A7<>
ENET_LINK_RXD<0>  13C5< 28C7>
ENET_LINK_RXD<7..0>  39A5>
ENET_LINK_RXD<1>  13C5< 28C7>
ENET_LINK_RXD<2>  13C5< 28C7>
ENET_LINK_RXD<3>  13C5< 28B7>
ENET_LINK_RXD<4>  13C5< 28B7>
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ENET_LINK_RXD<6>  13C5< 28B7>
ENET_LINK_RXD<7>  13C5< 28B7>
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ENET_LINK_TXD<7..0>  39A5>
ENET_LINK_TXD<1>  13B4< 13D5>
ENET_LINK_TXD<2>  13B4< 13D5>
ENET_LINK_TXD<3>  13B4< 13D5>
ENET_LINK_TXD<4>  13B4< 13D5>
ENET_LINK_TXD<5>  13B4< 13D5>
ENET_LINK_TXD<6>  13A4< 13D5>
ENET_LINK_TXD<7>  13A4< 13D5>
ENET_LINK_TX_EN  13D5<> 39A5>
ENET_LINK_TX_ER  13D5<> 39A5>
ENET_MDC           13C5> 28B7< 39A5>
ENET_MDIO          13C5<> 28B7<> 39A5>
ENET_PHY_TXD<0>  13B5< 28C7<
ENET_PHY_TXD<7..0>  39A5>
ENET_PHY_TXD<1>  13B5< 28C7<
ENET_PHY_TXD<2>  13B5< 28C7<
ENET_PHY_TXD<3>  13B5< 28C7<
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ENET_PHY_TXD<5>  13B5< 28C7<
ENET_PHY_TXD<6>  13A5< 28C7<
ENET_PHY_TXD<7>  13A5< 28C7<
ENET_PHY_TX_EN     13D6< 28C7< 39A5>
ENET_PHY_TX_ER     13D6< 28C7< 39A5>
ENET_RSET          28A5<
ENET_RST_L         28B7<
ENET_RX_DV         13D5< 28B7> 39A5>
ENET_RX_ER         13C5< 28B7> 39A5>
ENET_VSSC          28A7<>
ESP_EN_L           6C2<> 6C2<
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EXT_TMDS_D4_CMF  20A3<
EXT_TMDS_D5_CMF  20A3<
FAN1_GND           40B6> 41A3>
FAN1_PWM           27A4<>
FAN1_PWM_L         27A5<> 27B2<>
FAN1_TACH          27A4< 27B2< 41A3>
FAN2_GND           40B6> 41A3>
FAN2_PWM           27A3<>
FAN2_PWM_L         27A3<> 27B2<>
FAN2_TACH          27A3< 27B2< 41A3>
FB_4_85V_BU        33A5<
FP_PWR_EN          21C6<> 23A5< 23B3<>
FP_PWR_EN_L        23B3<>
FWB_TPB0           29A3<
FWB_TPB1           29A3<
FWPLL_BYP          29D8<>
FW_BIAS0           29A4<>
FW_BIAS1           29A4<>
FW_BMODE           29B6<
FW_CORE_ADJ        29C7<
FW_CORE_BYP        29C7<>
FW_CPS             29B6<
FW_GATE_EN         30D6<>
FW_GATE_EN_RC      30C6<>
FW_INPUT_PD        29A6<
FW_LINK_CNTL<0>  13C3<> 29C3<
FW_LINK_CNTL<1..0>  39A5>
FW_LINK_CNTL<1>  13C3<> 29C3<
FW_LINK_DATA<0>  13D3<> 29B7<
FW_LINK_DATA<7..0>  39A5>
FW_LINK_DATA<1>  13D3<> 29B7<
FW_LINK_DATA<2>  13D3<> 29B7<
FW_LINK_DATA<3>  13D3<> 29B7<
FW_LINK_DATA<4>  13C3<> 29B7<
FW_LINK_DATA<5>  13C3<> 29A7<
FW_LINK_DATA<6>  13C3<> 29A7<
FW_LINK_DATA<7>  13C3<> 29A7<
FW_LINK_LREQ       13C3<> 39A5>
FW_LKON            13C3<> 29B4<>
FW_OSC             29A4< 37A1>
FW_OSC_EN          29A3<
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FW_PC_PU           29B6<
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FW_PHY_CNTL<1..0>  39A5>
FW_PHY_CNTL<1>     29B4<> 29C4<
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FW_PHY_DATA<7..0>  39A5>
FW_PHY_DATA<1>     29B7<>
FW_PHY_DATA<2>     29B7<>
FW_PHY_DATA<3>     29B7<>
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FW_PHY_DATA<5>     29A7<>
FW_PHY_DATA<6>     29A7<>
FW_PHY_DATA<7>     29A7<>
FW_PHY_LPS         13C3<> 29B7<
FW_PHY_LREQ        13C2< 29B7< 39A5>
FW_PHY_PD          14C5<> 29B7<
FW_PHY_RESET_L     29A7<
FW_PINT            13C3<> 29B4> 39A5>
FW_PLL_ADJ         29C7<
FW_PORT1_SEL       29B6<
FW_POWER_UP        30C7<>
FW_R0              29A4<>
FW_R1              29A4<>
FW_TESTM           29A6<
FW_TPA1N           29B2<> 30A4<> 39D2>
FW_TPA1P           29B2<> 30A4<> 39D2>
FW_TPAO0N          30C2<> 39D2>
FW_TPAO0P          30C2<> 39D2>
FW_TPB1N           29A2<> 30A4<> 39D2>
FW_TPB1P           29B2<> 30A4<> 39D2>
FW_TPB2_PD         29A4<>
FW_TPBI0N          30C2<> 39D2>

FW_TPBI0P          30C2<> 39D2>
FW_TPI0N           29B2<> 30C3<> 39D2> 41A3>
FW_TPI0P           29B2<> 30C3<> 39D2> 41A3>
FW_TPI1N           30A3<> 39D2> 41D1>
FW_TPI1P           30A3<> 39D2> 41D1>
FW_TPO0N           29B2<> 30C3<> 39D2> 41A3>
FW_TPO0P           29B2<> 30C3<> 39D2> 41A3>
FW_TPO0R           30C1<> 41A3>
FW_TPO1N           30A3<> 39D2> 41D1>
FW_TPO1P           30A3<> 39D2> 41D1>
FW_VDD_ON          40A3>
FW_VGND            41A3> 41D1>
FW_VGND0           30C1<> 40A3>
FW_VGND1           30A3<> 40A3>
FW_VREG_PD         29A6<
FW_XI              29A4<> 37A1>
GPU_AGP_TEST       19C6<
GPU_B              21D6<> 23C8< 38A1>
GPU_C              21D6<> 23A8<
GPU_COMP           21D6<> 23A8<
GPU_CORE_OK        21A6<> 21D4<> 22D2<> 22D7<>
GPU_DVI_DDC_CLK  21C5<> 23D3<>
GPU_DVI_DDC_DATA  21C5<> 23C3<>
GPU_DVO_CLKP       19B3<
GPU_DVO_CLKP_R1  19B2< 20A8< 38C1>
GPU_DVO_CLKP_R2  19B2< 20A6< 38C1>
GPU_G              21D6<> 23C8< 38B1>
GPU_HPD            21C5< 23C3<>
GPU_MEM_IO         19A6<> 19B8< 22A7< 22B4< 22D2<
                 40C3>
GPU_MEM_IO_FLT     22C2< 40C3>
GPU_R              21D6<> 23B8< 38B1>
GPU_THERM_DM       19A6<> 27A6<
GPU_THERM_DP       19A6<> 27A6<
GPU_TV_GND1        23B8<> 40B6>
GPU_TV_GND2        23A8<> 40B6>
GPU_VCORE          19D8< 21B3<> 21B5<> 21D4< 40C3>
                 41C6>
GPU_VCORE_CNTL     21A3<>
GPU_VCORE_CNTL_L   21A4< 21B7<>
GPU_VCORE_CNTL_RC  21A3<>
GPU_VCORE_NECK     21B5<> 40B3>
GPU_VCORE_PWR_SEQ  21A8<>
GPU_VCORE_SEQ      21A8<
GPU_VCORE_SEQ_L    21A8<
GPU_VCORE_SW       21A4<> 40B1>
GPU_VCORE_SW_F     21A3<> 40B1>
GPU_VCORE_VDDCI    19C8< 19D6< 40B3>
GPU_Y              21D6<> 23B8<
HD_ADDR<0>         26C2<> 26C3<
HD_ADDR<2..0>      39C5>
HD_ADDR<1>         26C2<> 26C3<
HD_ADDR<2>         26B3< 26C1<>
HD_CS0_L           26C2<> 26C3< 39B5>
HD_CS1_L           26B3< 26C1<> 39B5>
HD_DATA<0>         26C2<> 26D3<
HD_DATA<15..0>     39C5>
HD_DATA<1>         26C2<> 26D3<
HD_DATA<2>         26D2<> 26D3<
HD_DATA<3>         26D2<> 26D3<
HD_DATA<4>         26C3< 26D2<>
HD_DATA<5>         26C3< 26D2<>
HD_DATA<6>         26C3< 26D2<>
HD_DATA<7>         26C3< 26D2<>
HD_DATA<8>         26C3< 26D1<>
HD_DATA<9>         26C3< 26D1<>
HD_DATA<10>        26C3< 26D1<>
HD_DATA<11>        26D1<> 26D3<
HD_DATA<12>        26B3< 26D1<>
HD_DATA<13>        26B3< 26D1<>
HD_DATA<14>        26C1<> 26C3<
HD_DATA<15>        26B3< 26C1<>
HD_DIOR_L          26A3< 26C2<> 39B5>
HD_DIOW_L          26A3< 26C1<> 39B5>
HD_DMACK_L         26A3< 26C2<> 39B5>
HD_DMARQ           13C6< 26C2<> 39B5>
HD_INTRQ           13C6< 26C1<> 39B5>
HD_IOCHRDY         26A3< 26C1<> 39B5>
HD_RESET_L         26A3< 26D2<> 39C5>
HIGH_VCORE         21A2<>
HIGH_VCORE_DIVD  21A3<
HPD_4V_REF         23C2<
HPD_PWR_SNS_EN     21C7<> 23C3<>
HPD_PWR_SW         23C1<
HPD_PWR_SW_BASE  23C2<>
HPD_REF_EN_L       23C2<>
IAC_FB             32D4<
IAC_RC_COMP        32D3<
ICT_TRST_L         6B2<> 6C2<
INTREPID_ACS_REF  8A5<
INT_AGPPVT         12D4<>
INT_AGP_FB_IN      12C4< 37C1>
INT_AGP_FB_OUT     12C4<> 37C1>
INT_AGP_VREF       12B5< 12D4<> 19D6< 40C3>
INT_CPUFB_IN       8A5< 8B5< 37D1>
INT_CPUFB_IN_NORM  8A4< 37D1>
INT_CPUFB_LONG     8A3< 37D1>
INT_CPUFB_OUT      8A5<> 8A5< 37D1>
INT_CPUFB_OUT_NORM  8A4< 37D1>
INT_CPUFB_OUT_SHORT  8A5< 37D1>
INT_DDRCLK2_N_TP  9B6<>
INT_DDRCLK2_P_TP  9B6<>
INT_DDRCLK5_N_TP  9B6<>
INT_DDRCLK5_P_TP  9B6<>
INT_ENET_RST_L     14B5<> 28B8<
INT_EXTINT3_PU     14A7<> 14B5<>
INT_EXTINT8_PU     14B5<> 14C7<
INT_EXTINT10_PU  14B5<> 14B7<
INT_EXTINT13_PU  14B5<> 14B7<
INT_EXTINT14_PU  14B5<> 14C7<
INT_EXTINT16_PU  14B5<> 14B7<
INT_GPIO1_PU       14B7< 14C5<> 35C8<
INT_GPIO9_PU       14B5<> 14B7<
INT_GPIO12_PU      14B5<> 14B7<
INT_GPIO15_PU      14B5<> 14B7<
INT_I2C_CLK0       6B3<> 6D2< 11A5<> 11A8<> 13C2<
                 13C3<> 24D7<> 41C6>
INT_I2C_CLK1       13C2< 13C3<> 14B7< 24B3<> 25C2<>
                 27B4< 41C6>
INT_I2C_CLK2       14A2<> 27D7<> 41A6>
INT_I2C_DATA0      6B3<> 6D2<> 11A5<> 11A8<> 13C2<
                 13C3<> 24D7<> 41C6>
INT_I2C_DATA1      13B2< 13C3<> 14B7< 24B3<> 25C2<>
                 27B4<> 41C6>
INT_I2C_DATA2      14A2<> 27D7<> 41A6>
INT_I2S0_SND_FROM_ADC  14B2< 27D7<> 41A6>
INT_I2S0_SND_LRCLK  14B1< 27D8<> 41A6>
INT_I2S0_SND_LRCLK_UF  14A3<>
INT_I2S0_SND_MCLK  14B1< 27D8<> 37B1> 41A6>
INT_I2S0_SND_MCLK_UF  14A3<>
INT_I2S0_SND_SCLK  14B1< 27D7<> 41A6>
INT_I2S0_SND_SCLK_UF  14A3<>
INT_I2S0_SND_TO_DAC  14B1< 27D8<> 41A6>
INT_I2S0_SND_TO_DAC_UF  14B3<>
INT_JTAG_TEI       13C2< 13C5< 41D6>
INT_MEM_REF_H      9B6< 40C3>
INT_MEM_VREF       9A7< 9B6<> 40C3>
INT_MOD_BITCLK     14A1< 27C3<
INT_MOD_BITCLK_UF  14A3<> 14A7<
INT_MOD_CLKOUT     14A1< 27C3<
INT_MOD_CLKOUT_UF  14A3<> 14A7<
INT_MOD_DTI        14A2< 14A7< 27C3<
INT_MOD_DTO        14B1< 27C3<
INT_MOD_DTO_UF     14A3<> 14A7<
INT_MOD_SYNC       14A1< 27C3<
INT_MOD_SYNC_UF    14A3<> 14A7<
INT_PCI_FB_IN      12C7< 37C1>
INT_PCI_FB_OUT     12C7<> 37C1>
INT_PEND_PROC_INT  14A5> 31C4<>
INT_PROC_SLEEP_REQ_L  14A5< 31B4<>
INT_PU_RESET_L     13D3< 27D5<> 31A2< 31C4<>
INT_REF_CLK_IN     14A5< 14B5< 37C1>
INT_REF_CLK_OUT    14A5< 14B7< 37C1>
INT_REF_CLK_OUT_UF  14A5<> 37C1>
INT_RESET_L        9B3< 13D3< 31C7< 31D4<>
INT_ROM_CS_L       12A5< 12C7>
INT_ROM_OE_L       12A5< 12C7>
INT_ROM_RW_L       12A5< 12C7>
INT_SUSPEND_ACK_L  8B5> 31B6<>
INT_SUSPEND_REQ_L  8B5< 31B6<> 31C7<
INT_TDO            13C5> 13D2< 14A6< 28A5<
INT_TST_MONIN_PD  13C2< 13C5< 41C6>
INT_TST_MONOUT_TP  13C5> 41C6>
INT_TST_PLLEN_PD  13C5< 13D2< 41C6>
INT_WATCHDOG_L     14A5> 31C6<>
INV_GND            23A1<> 41A6>
INV_ON_PWM         21C6<> 23A3<

IO_RESET_L         17A8< 24D7<> 25C2< 28B8< 31C6<>
                 31D7<
JTAG_ASIC_TCK      13C5< 13D2< 28A5< 41D6>
JTAG_ASIC_TDI      13C5< 13D2< 41D6>
JTAG_ASIC_TDO_TP  28A5> 41D6>
JTAG_ASIC_TMS      13C5< 13D2< 28A5< 41D6>
JTAG_ASIC_TRST_L  13C2< 13C5< 28A5< 41D6>
JTAG_CPU_TCK       5A2< 5B3< 6A3< 41D6>
JTAG_CPU_TDI       5B2< 5C3< 6B2<> 41D6>
JTAG_CPU_TDO_TP  5C3> 41D6>
JTAG_CPU_TMS       5B2< 5B3< 6B2<> 41D6>
JTAG_CPU_TRST_L  5B3< 6A4< 6B2<> 41D6>
KBDLED_ANODE       24B3<> 24D7<>
KBDLED_RETURN      24B3<> 24D7<>
KBD_CAPSLOCK_LED  41B3>
KBD_COMMAND_L      24C2< 31C6<> 41B3>
KBD_CONTROL_L      24C2< 31C6<> 41A3>
KBD_FUNCTION_L     24C2< 31B6<> 41B3>
KBD_ID             24D2< 31B6<> 41B3>
KBD_INTL           41B3>
KBD_JIS            41B3>
KBD_NUMLOCK_LED  41B3>
KBD_OPTION_L       24C2< 31B6<> 41B3>
KBD_SHIFT_L        24C2< 31C6<> 41A3>
KBD_X<0>           24D2< 31C6<>
KBD_X<0..9>        41A3>
KBD_X<1>           24D2< 31C6<>
KBD_X<2>           24C2< 31C6<>
KBD_X<3>           24C2< 31C6<>
KBD_X<4>           24C2< 31C6<>
KBD_X<5>           24C2< 31C6<>
KBD_X<6>           24C2< 31C6<>
KBD_X<7>           24C2< 31C6<>
KBD_X<8>           24C2< 31C6<>
KBD_X<9>           24C2< 31C6<>
KBD_Y<0..7>        41A3>
LCD_DIGON_L        23B6<
LCD_PWREN_L        23B5<>
LED_LINK10         28B5<>
LED_LINK100        28B5<>
LED_RX_SPN         28B5>
LID_CLOSED_L       24A3<> 41C1>
LM2594_IN          29D8<> 40A3>
LMU_DETECT         24C7< 24D6<> 41D1>
LT1962_INT_ADJ     14D7<
LT1962_INT_BYP     14D7<>
LTC1625_ITH        32D2<>
LTC1962_INT_VIN  14D8<> 40A1>
LTC3405_SW         28D4<> 40A3>
LTC3411_EN_L       36A7<
LTC3411_GND        36A5<> 40A1>
LTC3411_ITH        36A5<> 40A1>
LTC3411_ITH_RC     36A5< 40A1>
LTC3411_SHDN       36A6<> 40A1>
LTC3411_SYNC       36A6<> 40A1>
LTC3411_VCC        36A6< 36A7< 40B1>
LTC3707_START_RC  34B6<
LUX_ALS_GAIN_SW  24B8<> 24D6<>
LUX_ALS_OUT        24B8<> 24D6<>
LVDS_DDC_CLK       21C5<> 23A4< 23B4<> 41B6>
LVDS_DDC_DATA      21C5<> 23A4< 23B4<> 41B6>
LVDS_L0N           21B5> 23B4<> 39C2> 41B6>
LVDS_L0P           21B5> 23B4<> 39C2> 41B6>
LVDS_L1N           21B5> 23B4<> 39C2> 41B6>
LVDS_L1P           21B5> 23B4<> 39C2> 41B6>
LVDS_L2N           21B5> 23A4<> 39C2> 41B6>
LVDS_L2P           21B5> 23A4<> 39C2> 41B6>
LVDS_L3N_TP        21B5>
LVDS_L3P_TP        21B5>
LVDS_U0N           39C2>
LVDS_U0P           39C2>
LVDS_U1N           39C2>
LVDS_U1P           39C2>
LVDS_U2N           39C2>
LVDS_U2P           39C2>
MAIN_RESET_L       14C7< 17A8< 18A7< 19B8< 20B6<
                 26D6<> 31D4<> 31D7< 41C3>
MASTER_SWING       20B7< 20D6<
MAX1715_GND        36B5<> 36C5< 40C1>
MAX1715_ON_RC      36C7<>
MAX1715_REF        36B5<> 40C1>
MAX1715_SKIP       36C4< 40C1>
MAX1715_TON        36C5< 40C1>
MAX1715_VCC        36D5< 40C1>
MAX4172_OUT        32D4<>
MAXBUS_SLEEP       5D2< 5D5< 6A3< 6B2< 6B4< 7B7< 7D8<
                 8B3< 8B8< 8C8< 8D1< 8D8< 15D8< 16D8<
                 35D8< 40D3>
MDI0_PD            28B4<
MDI1_PD            28B4<
MDI2_PD            28B4<
MDI3_PD            28B3<
MDI_M<0>           28B5<> 39D2>
MDI_M<0..3>        41A3>
MDI_M<1>           28B5<> 39D2>
MDI_M<2>           28B5<> 39C2>
MDI_M<3>           28B5<> 39C2>
MDI_P<0>           28B5<> 39D2>
MDI_P<0..3>        41A3>
MDI_P<1>           28B5<> 39D2>
MDI_P<2>           28B5<> 39C2>
MDI_P<3>           28B5<> 39C2>
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MEM_ADDR<12..0>  37A5>
MEM_ADDR<1>        9B5< 9D6<>
MEM_ADDR<2>        9B5< 9D6<>
MEM_ADDR<3>        9B5< 9D6<>
MEM_ADDR<4>        9B5< 9D6<>
MEM_ADDR<5>        9B5< 9D6<>
MEM_ADDR<6>        9B5< 9D6<>
MEM_ADDR<7>        9B5< 9D6<>
MEM_ADDR<8>        9B5< 9D6<>
MEM_ADDR<9>        9A5< 9D6<>
MEM_ADDR<10>       9A5< 9D6<>
MEM_ADDR<11>       9A5< 9D6<>
MEM_ADDR<12>       9A5< 9D6<>
MEM_BA<0>          9A5< 9D6<>
MEM_BA<1..0>       37A5>
MEM_BA<1>          9A5< 9C6<>
MEM_CAS_L          9A5< 9C6<> 37A5>
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MEM_CKE<3..0>      37A5>
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MEM_CKE<2>         9B6<> 9C5<
MEM_CKE<3>         9B6<> 9C5<
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MEM_CS_L<3..0>     37A5>
MEM_CS_L<1>        9C5< 9C6<>
MEM_CS_L<2>        9C5< 9C6<>
MEM_CS_L<3>        9C5< 9C6<>
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MEM_DATA<7..0>     37D5>
MEM_DATA<1>        9D8<> 10C7<>
MEM_DATA<2>        9D8<> 10C7<>
MEM_DATA<3>        9D8<> 10C7<>
MEM_DATA<4>        9D8<> 10C7<>
MEM_DATA<5>        9D8<> 10C7<>
MEM_DATA<6>        9D8<> 10C7<>
MEM_DATA<7>        9D8<> 10C7<>
MEM_DATA<8>        9D8<> 10C7<>
MEM_DATA<15..8>  37D5>
MEM_DATA<9>        9D8<> 10C7<>
MEM_DATA<10>       9D8<> 10C7<>
MEM_DATA<11>       9D8<> 10C7<>
MEM_DATA<12>       9D8<> 10B7<>
MEM_DATA<13>       9C8<> 10B7<>
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MEM_DATA<16>       9C8<> 10C5<>
MEM_DATA<23..16>  37C5>
MEM_DATA<17>       9C8<> 10C5<>
MEM_DATA<18>       9C8<> 10C5<>
MEM_DATA<19>       9C8<> 10C5<>
MEM_DATA<20>       9C8<> 10C5<>
MEM_DATA<21>       9C8<> 10C5<>
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MEM_DATA<23>       9C8<> 10C5<>
MEM_DATA<24>       9C8<> 10C5<>
MEM_DATA<31..24>  37C5>
MEM_DATA<25>       9C8<> 10C5<>
MEM_DATA<26>       9C8<> 10C5<>
MEM_DATA<27>       9C8<> 10C5<>
MEM_DATA<28>       9C8<> 10C5<>
MEM_DATA<29>       9C8<> 10B5<>
MEM_DATA<30>       9C8<> 10B5<>
MEM_DATA<31>       9C8<> 10B5<>
MEM_DATA<32>       9C8<> 10C3<>
MEM_DATA<39..32>  37C5>

MEM_DATA<33>       9C8<> 10C3<>
MEM_DATA<34>       9C8<> 10C3<>
MEM_DATA<35>       9C8<> 10C3<>
MEM_DATA<36>       9C8<> 10C3<>
MEM_DATA<37>       9C8<> 10C3<>
MEM_DATA<38>       9C8<> 10C3<>
MEM_DATA<39>       9B8<> 10C3<>
MEM_DATA<40>       9B8<> 10C3<>
MEM_DATA<47..40>  37B5>
MEM_DATA<41>       9B8<> 10C3<>
MEM_DATA<42>       9B8<> 10C3<>
MEM_DATA<43>       9B8<> 10C3<>
MEM_DATA<44>       9B8<> 10C3<>
MEM_DATA<45>       9B8<> 10B3<>
MEM_DATA<46>       9B8<> 10B3<>
MEM_DATA<47>       9B8<> 10B3<>
MEM_DATA<48>       9B8<> 10C1<>
MEM_DATA<55..48>  37B5>
MEM_DATA<49>       9B8<> 10C1<>
MEM_DATA<50>       9B8<> 10C1<>
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MEM_DATA<52>       9B8<> 10C1<>
MEM_DATA<53>       9B8<> 10C1<>
MEM_DATA<54>       9B8<> 10C1<>
MEM_DATA<55>       9B8<> 10C1<>
MEM_DATA<56>       9B8<> 10C1<>
MEM_DATA<63..56>  37A5>
MEM_DATA<57>       9B8<> 10C1<>
MEM_DATA<58>       9B8<> 10C1<>
MEM_DATA<59>       9B8<> 10C1<>
MEM_DATA<60>       9B8<> 10C1<>
MEM_DATA<61>       9B8<> 10B1<>
MEM_DATA<62>       9B8<> 10B1<>
MEM_DATA<63>       9B8<> 10B1<>
MEM_DQM<0>         9C6<> 10C7<> 37D5>
MEM_DQM<1>         9C6<> 10B7<> 37D5>
MEM_DQM<2>         9C6<> 10C5<> 37C5>
MEM_DQM<3>         9C6<> 10B5<> 37C5>
MEM_DQM<4>         9C6<> 10C3<> 37B5>
MEM_DQM<5>         9C6<> 10B3<> 37B5>
MEM_DQM<6>         9C6<> 10C1<> 37B5>
MEM_DQM<7>         9C6<> 10B1<> 37A5>
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MEM_DQS<2>         9C6<> 10C5<> 37C5>
MEM_DQS<3>         9C6<> 10B5<> 37C5>
MEM_DQS<4>         9C6<> 10C3<> 37B5>
MEM_DQS<5>         9C6<> 10B3<> 37B5>
MEM_DQS<6>         9C6<> 10C1<> 37B5>
MEM_DQS<7>         9C6<> 10B1<> 37A5>
MEM_MUXSEL_LSB     9B6<> 10B5<> 10B7<> 37A5>
MEM_MUXSEL_LSB_L_TP  9B6<>
MEM_MUXSEL_MSB     9B6<> 10B1<> 10B3<> 37A5>
MEM_MUXSEL_MSB_L_TP  9B6<>
MEM_RAS_L          9A5< 9C6<> 37A5>
MEM_WE_L           9A5< 9C6<> 37A5>
MMM_ACC_DETECT     25B8<> 25C2<>
MMM_ACC_PWRDOWN    25B8<> 25C1< 25C7<>
MMM_ACC_SELFTEST   25B8<> 25C2<> 25C7<> 41C1>
MMM_ACC_X_AXIS     25C5> 25C6< 25D2<> 41C1>
MMM_ACC_Y_AXIS     25B6< 25C2<> 25C5> 41C1>
MMM_ACC_Z_AXIS     25B6< 25C2<> 25C5> 41C1>
MMM_FFIRQ_L        14A6< 14B5<> 25C1<
MMM_PIC_AAC_PWRDOWN  25C2<>
MMM_PIC_AN2_PD     25C4<>
MMM_PIC_AN3_PU     25C4<>
MMM_PIC_FFIRQ_L    25C2<>
MMM_PIC_SIRQ_L     25C2<>
MMM_RESET_L        25C1< 25C2<>
MMM_SIRQ_L         14A6< 14B5<> 25C1<
MPIC_CPU_INT_L     5B2< 5B3< 14B5>
MSEN_M             20B7> 20D7<
MSEN_S             20B4> 20D6<
NEC_AMC_TP         17A5<
NEC_AVDD           17D6< 40A3>
NEC_AVSS_F         17A5< 17B4<
NEC_CRUN_L         17A7<>
NEC_IDSEL          17B7<
NEC_IO_RESET_L     17A7< 17B7<
NEC_LEGC           17A7< 17A8<
NEC_LUSB_OCI       17B3< 17B5<
NEC_LUSB_OCI_UF    17B1< 27D8<> 41A6>
NEC_LUSB_PPON      17B5> 27D8<> 41A6>
NEC_MAIN_RESET_L  17A7< 17A7<
NEC_NANDTESTEN_TP  17A4<
NEC_NANDTESTOUT_TP  17A4<>
NEC_NC<1>          17B5<>
NEC_NC<2>          17B5<>
NEC_OCI<3>         17B5<
NEC_OCI<4>         17B5<
NEC_OCI<5>         17B5<
NEC_PCI_GNT_L      12C7<> 17B7<
NEC_PCI_INTA_L     17B7<>
NEC_PCI_INTB_L     17B7<>
NEC_PCI_INTC_L     17B7<>
NEC_PCI_INT_L      14B5<> 14D7< 17B8<
NEC_PCI_REQ_L      12A7< 12D7<> 17B7>
NEC_PME_L          17A7> 17A7<
NEC_PPON3_TP       17B5>
NEC_PPON4_TP       17B5>
NEC_PPON5_TP       17B5>
NEC_RREF           17B5<>
NEC_RUSB_OCI       17B3< 17B5<
NEC_RUSB_OCI_UF    17B1< 27D1<> 41D3>
NEC_RUSB_PPON      17B5> 27D1<> 41D3>
NEC_SMI_L_TP       17A7>
NEC_USB_DAM        17D2<> 27D7<> 39B2> 41D3>
NEC_USB_DAP        17D2<> 27D7<> 39B2> 41D3>
NEC_USB_DBM        17C2<> 27D2<> 39B2> 41D3>
NEC_USB_DBP        17C2<> 27D2<> 39B2> 41D3>
NEC_USB_RSDM1      17C5<>
NEC_USB_RSDM2      17C5<>
NEC_USB_RSDP1      17C5<>
NEC_USB_RSDP2      17C5<>
NEC_XT1            17D5<
NEC_XT2            17D5<>
NEC_XT2_R          17D4<
OVER_18V_ADJ       32C3<>
PCI1510_VR_EN_L    18C7<
PCI_AD<0>          9C3< 12D6<> 17D7<> 18C7<> 26B5<>
PCI_AD<31..0>      39C5> 41D3>
PCI_AD<1>          9C3< 12D6<> 17D7<> 18C7<> 26B6<>
PCI_AD<2>          9C3< 12D6<> 17D7<> 18C7<> 26C5<>
PCI_AD<3>          9C3< 12D6<> 17C7<> 18C7<> 26C6<>
PCI_AD<4>          9C3< 12D6<> 17C7<> 18C7<> 26C5<>
PCI_AD<5>          9C3< 12D6<> 17C7<> 18C7<> 26C6<>
PCI_AD<6>          9C3< 12C6<> 17C7<> 18C7<> 26C5<>
PCI_AD<7>          9C3< 12C6<> 17C7<> 18C7<> 26C6<>
PCI_AD<8>          9C3< 12C6<> 17C7<> 18C7<> 26C6<>
PCI_AD<9>          9C3< 12C6<> 17C7<> 18C7<> 26C5<>
PCI_AD<10>         9C3< 12C6<> 17C7<> 18C7<> 26C6<>
PCI_AD<11>         9C3< 12C6<> 17C7<> 18C7<> 26C5<>
PCI_AD<12>         9C3< 12C6<> 17C7<> 18C7<> 26C6<>
PCI_AD<13>         9C3< 12C6<> 17C7<> 18C7<> 26C5<>
PCI_AD<14>         9C3< 12C6<> 17C7<> 18C7<> 26C6<>
PCI_AD<15>         9C3< 12C6<> 17C7<> 18C7<> 26C5<>
PCI_AD<16>         9C3< 12C6<> 17C7<> 18C7<> 26C5<>
PCI_AD<17>         9C3< 12C6<> 17C7<> 18C7<> 26C6<>
PCI_AD<18>         9C3< 12C6<> 17C7<> 18B7<> 26C5<>
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PCI_AD<19>         9B3< 12C6<> 17C7<> 18B7<> 26C6<>
PCI_AD<20>         9B3< 12C6<> 17C7<> 18B7<> 26C5<>
PCI_AD<21>         12C6<> 17C7<> 18B7<> 26C6<>
PCI_AD<22>         12C6<> 17C7<> 18B7<> 26C5<>
PCI_AD<23>         12C6<> 17C7<> 18B7<> 26C6<>
PCI_AD<24>         9C1<> 12C6<> 17C7<> 18B7<> 26C5<>
PCI_AD<25>         9C1<> 12C6<> 17C7<> 18B7<> 26C6<>
PCI_AD<26>         9C1<> 12C6<> 17C7<> 18B7<> 26C5<>
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PCI_AD<28>         9C1<> 12C6<> 17C7<> 18B7<> 26C5<>
PCI_AD<29>         9C1<> 12C6<> 17B7<> 18B7<> 26D6<>
PCI_AD<30>         9C1<> 12C6<> 17B7<> 18B7<> 26D5<>
PCI_AD<31>         9C1<> 12C6<> 17B7<> 18B7<> 26D6<>
PCI_CBE<0>         12C7<> 17B7<> 18B7<> 26C5<>
PCI_CBE<3..0>      39C5>
PCI_CBE<1>         12C7<> 17B7<> 18B7<> 26C6<>
PCI_CBE<2>         12C7<> 17B7<> 18B7<> 26C6<>
PCI_CBE<3>         12C7<> 17B7<> 18B7<> 26C6<>
PCI_DEVSEL_L       12B7< 12C7<> 17B7<> 18A7<> 26C5<>
                 39C5> 41C3>
PCI_FRAME_L        12B7< 12C7<> 17B7<> 18B7<> 26C5<>
                 39C5> 41D3>
PCI_IRDY_L         12B7< 12C7<> 17B7<> 18B7<> 26C6<>
                 39C5> 41D3>
PCI_PAR            12C7<> 17B7<> 18B7<> 26C5<> 39C5>
                 41C3>
PCI_PERR_L         17B7<> 18B7<> 18D7<
PCI_SERR_L         17B7> 18B7> 18D7<
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                  39C5> 41C3>
PCI_TRDY_L        12B7< 12C7<> 17B7<> 18A7<> 26C5<>
                  39C5> 41D3>
PLL_STOP_L        7C4<> 7C8<>
PMU_ACK_L         14C2< 31C4<>
PMU_AC_DET        31A5< 31B4<>
PMU_AC_IN         31B4<>
PMU_BATT0_DET_L   31B4<>
PMU_BATT1_DET_L_PU  31B4<> 31D2<
PMU_BATT_DET_L    31A4<> 31B3< 31D2< 32A4<> 41A3>
PMU_BYTE          31B6< 31C7<
PMU_CHARGE_V      31C4<> 32B8<>
PMU_CHRG_BATT_B   31C4<> 32A8<>
PMU_CLK           14C2<> 31C4<>
PMU_CNVSS         31B6< 31C7<
PMU_CPU_HRESET_L  6A2< 6C3<> 31C4<> 41C1>
PMU_CUSTOM_RESET  31A7<> 31B8<
PMU_CUSTOM_RESET_L  31A8<>
PMU_EPM           31C4<> 31D2<
PMU_FROM_INT      14C2<> 31C4<>
PMU_I2C_CLK       31B4<> 31C2<
PMU_I2C_DATA      31B4<> 31C2<
PMU_INT_L         14B5<> 14B7< 31B6<>
PMU_INT_NMI       14B5<> 14B7< 31D4<>
PMU_KB_RESET_L    41C1>
PMU_LID_CLOSED_L  24A1< 24D6<> 31B2< 31C4<> 41D1>
PMU_MMI_BUTTON_L  31C2< 31C4<>
PMU_MMI_L         31C2< 31C4<>
PMU_OOPS          31B2< 31B4<>
PMU_PME_L         14A5<> 17A8< 26D5<> 31B2< 31C4<>
                  41C3>
PMU_POWERUP_OK    31B4<> 31D2<
PMU_POWER_UP_L    30C8<> 31C6<> 31D7< 34B8<
PMU_RBQ_L         14B7< 14C2> 31C4<>
PMU_RESET_BUTTON_L  24A7< 31C4<> 31D2<
PMU_RESET_L       31B6< 31B7>
PMU_SELECT        31C6>
PMU_SLEEP_LED     24C7<> 24D6<> 41D1>
PMU_SLEEP_LED_L   24C6<> 31C4<>
PMU_SMB_CLK       31B4<> 31C2< 32A3<
PMU_SMB_DATA      31B4<> 31C2< 32A2<
PMU_TO_INT        14C2<> 31C4<>
POWER_UP          30D7<>
POWER_VALID       31B2< 31C4<>
P3V3_MMM          25C8< 25D5<
PP3V3_MMM_PIC     25C1< 25D5<
PP3V3_SI_AVCC1    20C7< 20D7<
PP3V3_SI_AVCC2    20C5< 20D7<
PP3V3_SI_PVCC1    20C7<
PP3V3_SI_PVCC2    20C5<
PP3V3_SI_VCC1     20C7< 20D8<
PP3V3_SI_VCC2     20C5< 20D7<
PWR_BUTTON_L      24A7< 24B3<>
RAM_ADDR<0>       9B4< 11B3<> 11B6<>
RAM_ADDR<12..0>   37A5>
RAM_ADDR<1>       9B4< 11B5<> 11B8<>
RAM_ADDR<2>       9B4< 11B3<> 11B6<>
RAM_ADDR<3>       9B4< 11B5<> 11B8<>
RAM_ADDR<4>       9B4< 11B3<> 11B6<>
RAM_ADDR<5>       9B4< 11B5<> 11B8<>
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RAM_ADDR<7>       9B4< 11B5<> 11B8<>
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RAM_CS_L<3..0>    37A5>
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RAM_DATA_A<7..0>  37D5>
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RAM_DATA_A<6>     10B8<> 11D8<>
RAM_DATA_A<7>     10B8<> 11D8<>
RAM_DATA_A<8>     10B8<> 11D8<>
RAM_DATA_A<15..8>  37C5>
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RAM_DATA_A<10>    10C7<> 11D8<>
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RAM_DATA_A<23..16>  37C5>
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RAM_DATA_B<10>    10C8<> 11D5<>
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RAM_DATA_B<23..16>  37C5>
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ROM_OE_L          9B3< 12A4< 41C3>
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ROM_ONBOARD_CS_TP_L  9B3< 26C6<>
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SI_RESET_L        20B6< 21C7<>
SI_RESET_L_R      20B4< 20B7< 20D7<
SI_SECONDARY      20A6< 20D7<
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SND_HW_RESET_L    14A8< 14B5<> 27D7<> 41A6>
SND_LIN_SENSE_L   14B5<> 27C8<> 41A6>
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SYSCLK_DDRCLK_A0_L  9D4< 11D8<> 37C1>
SYSCLK_DDRCLK_A0_L_UF  9B6<> 9D5< 37D1>
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SYSCLK_DDRCLK_A1  9D4< 11A6<> 37C1>
SYSCLK_DDRCLK_A1_L  9D4< 11A6<> 37C1>
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SYSCLK_DDRCLK_B0_L  9C4< 11D5<> 37C1>
SYSCLK_DDRCLK_B0_L_UF  9B6<> 9C5< 37D1>
SYSCLK_DDRCLK_B0_UF  9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_B1  9D4< 11A3<> 37C1>
SYSCLK_DDRCLK_B1_L  9D4< 11A3<> 37C1>
SYSCLK_DDRCLK_B1_L_UF  9B6<> 9D5< 37D1>
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THERM2_A_DP       27A7< 27A8< 39A2>
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TMDS_CONN_CLKP    23C6<> 23C7<> 38C1> 41C6>
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TPS2211_SHTDWN_L  18C5<
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TV_Y              23A6<> 41A6>
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D	051-6680	B
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*** Part Cross-Reference for the entire design ***

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J3	CON_M40ST_D4MT_SM	27
J4	CON_4RT_WRIB	23
J5	CON_M80ST_D4MT_SM	18
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J8	CON_2RTSM_125	24
J9	CON_F1ST_S2MT_SM	14
J10	CON_M16ST_D_SMA	24
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J15	CON_F10RT_S2MT_SM	27
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J17	CON_M16ST_D_SMA	27
J18	CON_M4RT_S2MT_SM	27
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J20	CON_F9RT_1394B_S6MT_SMA	30
J21	CON_F5RT_MINIDIN_TH	23
J22	CON_F30RT_T6MT_TH1	23
J23	CON_RJ45_10RT_S4MT_TH1	28
J24	CON_F6RT_S4MT_TH1	30
J25	CON_F400RT_DDRDIMM_SM3	11
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J28	CON_10STSM_5087	27
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RP3	RPAK4P	8
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RP5	RPAK4P	14
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RP35	RPAK4P	13
RP36	RPAK4P	12
RP37	RPAK4P	29
RP38	RPAK4P	29
RP39	RPAK4P	31
RP40	RPAK10P2C	24

RP41	RPAK4P	31
RP42	RPAK10P2C	24
RP43	RPAK4P	17
RP44	RPAK4P	17
RP45	RPAK4P	17
RP46	RPAK10P2C	6
RP47	RPAK4P	14
RP61	RPAK2P	20
RP70	RPAK2P	20
RP72	RPAK2P	20
RP74	RPAK2P	20
RP75	RPAK2P	20
SH1	SHLD_3P_EMI	4
U1	COMPARATOR_LMC7211	32
U2	NC7S32	23
U3	AMP_MAX4172	32
U4	PWR_CNTRL_TPS2211	18
U5	FAN2558	5
U6	MAX1772	32
U7	MAX1717	35
U8	PCI1510GGU	18
U9	SN74AUC1G08	6
U10	SN74AUC1G08	6
U11	FEPR_1MX8	9
U12	SN74AUC1G04	7
U13	LTC1625	33
U14	COMPARATOR_LMC7211	33
U15	PIC16F818_QFN	25
U16	CBTV4020	10
U17	UPD72810I_FBGA	17
U18	CBTV4020	10
U19	MAX1715	36
U20	KXM52	25
U21	74112S	24
U22	VREG_LP2951	33
U23	VREG_LP2951	33
U24	SIL178	20
U25	SIL178	20
U26	MAX6804	31
U27	CBTV4020	10
U28	CBTV4020	10
U29	M16C62	31
U30	CLK_GEN_CY25811	19
U31	CLK_GEN_CY28512	14
U32	LTC1778	21
U33	COMPARATOR_LMC7211	31
U34	VREG_MM1571J	22
U35	LTC3707	34
U36	TSB81BA3A	29
U37	VREG_LM2594	29
U38	VREG_LT1962	29
U39	74LG32	23
U40	74LG32	23
U41	INA138	25
U42	COMPARATOR_LMC7211	23
U43	TRANSCEIVER_88E1111	28
U44	LTC1761	29
U45	LTC3405	28
U46	LTC3411	36
U47	RAGE_MBLTY_M11_CSP64_667	19 21 22
U48	TRA_SI5467BDQ	36
U49	VREG_LT1962	14
U50	TRA_SI3447DV	36
U51	INTREPID	8 9 12 13 14 15
U52	EEPROM_32KX8_M24256B	6
U53	ADT7467	27
U54	ATTINY2313	6
U55	OPAMP_LMC7111	32
U56	APOLLO_MPC7447A_360	5 6
U57	COMPARATOR_LMC7211	32
U58	LIS3L02AQ	25
U59	COMPARATOR_LMC7211	30
U60	VREG_MM1571J	22
XW1	SHORT	32
XW2	SHORT	35
XW3	SHORT	33
XW4	SHORT	21
XW5	SHORT	21
XW6	SHORT	21
XW7	JUMPER	21
XW8	SHORT	36
XW9	SHORT	21
XW10	SHORT	36
XW11	SHORT	21
XW12	SHORT	21
XW13	SHORT	34
XW14	SHORT	23
XW15	SHORT	23
XW16	JUMPER	22
XW17	SHORT	36
XW18	JUMPER	26
XW19	JUMPER	33
XW20	JUMPER	34
XW21	SHORT	36
XW22	JUMPER	34
XW23	SHORT	36
XW24	JUMPER	36
XW25	SHORT	36
XW26	JUMPER	36
XW27	SHORT	35
XW28	SHORT	35
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XW32	SHORT	34
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XW37	SHORT	25
Y1	CRYSTAL	17
Y2	CRYSTAL	14
Y3	CRYSTAL_4PIN	31
Y4	CRYSTAL	31
Y5	CRYSTAL_4PIN	28
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